Intel® Open Source HD Graphics Programmers' Reference Manual (PRM)

Volume 4: Configurations

For the 2014-2015 Intel Atom™ Processors, Celeron™ Processors and Pentium™ Processors based on the "Cherry Trail/Braswell" Platform
(Cherryview/Braswell graphics)

October 2015, Revision 1.1

Creative Commons License

Notices and Disclaimers

Table of Contents

Configurations Overview

The Intel "Gen" Graphics Architecture was first introduced to the market in 2004. Since that time, the architecture and its implementation have evolved to add many new features, increase performance, and improve power efficiency.

Configurations

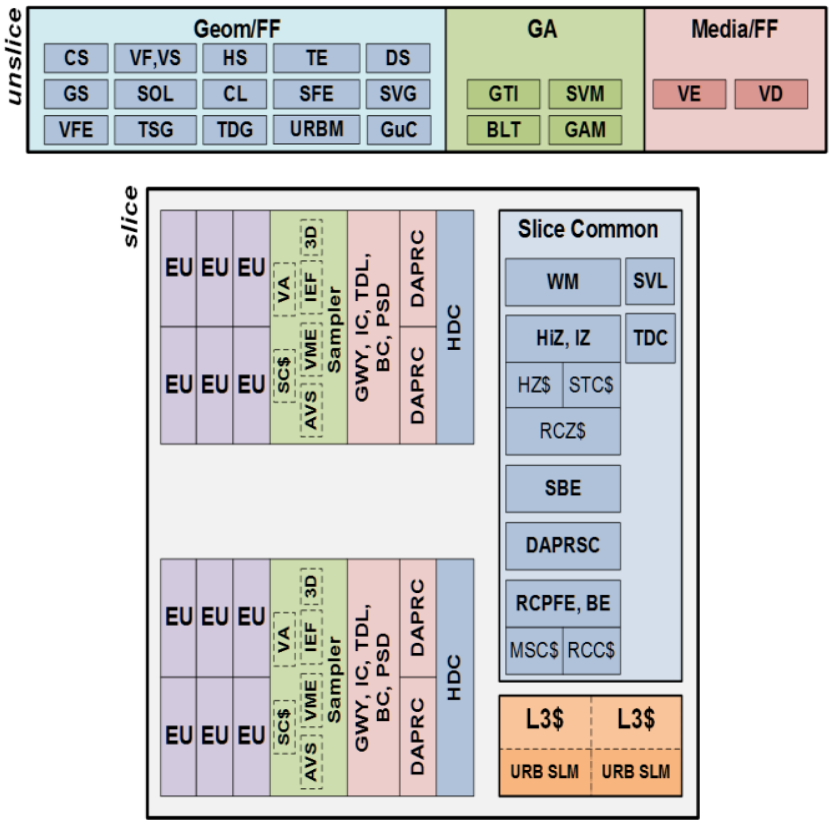
This chapter contains configurations details as described in the following sections:

- Top Level Block Diagrams
- Device Attributes
- Steppings & Device IDs

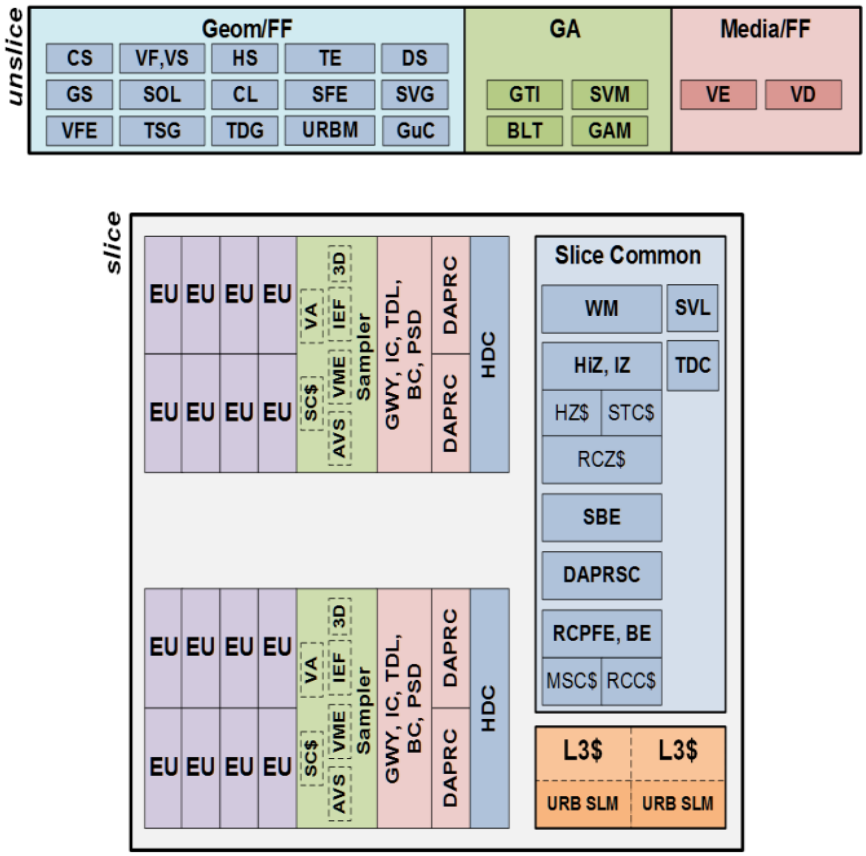
Top Level Block Diagrams

The diagram below shows basic feature blocks of the Cherryview (CHV) and Braswell (BSW) graphics architecture:

12 EU (2x6) Configuration:



16 EU (2x8) Configuration:



The above diagrams are based on the following functional partitions:

(a) Geometry Fixed Functions (Geom/FF)

(b) Media Fixed Functions (Media/FF)

(c) Global Assets and GT Interface (GA)

(d) One or more Subslices (two shown)

(e) A Slice Common block

(f) An L3 Cache (L3$) block

Note that the combination of (a), (b), and (c) is typically referred to as the “unslice”, while a combination of (d), (e), and (f) is referred to as a compute “slice”.

The functionality in each of these groupings is further broken down as follows:

- Unslice – Fixed function pipelines for 3D, GPGPU, and Media operations, and interface to the outside world.
  - The 3D Geometry / Fixed Function (Geom/FF) block consisting of:
    - 3D fixed function pipeline (CS, VFVS, HS, TE, DS, GS, SOL, SL, SFE, SVG)
    - Video Front-End unit (VFE)
    - Thread Spawner unit (TSG) and the global Thread Dispatcher unit (TDG)

        - Unified Return Buffer Manager (URBM)
    - Media fixed function assets:
        - Video Decode (VD) Box
        - Video Encode (VE) Box
        - Wireless Display (WD) BOX
    - The Global Assets (GA) block as the primary interface and memory stream gateway to the outside world, consisting of:
        - GT Interface (GTI)
        - State Variable Manager (SVM)
        - Blitter (BLT)
        - Graphics Arbiter (GAM)
- Subslice (three shown) – A compute unit with supporting fixed- or shared-function assets sufficient for the EU capability.
    - A bank of Execution Units (EUs) – eight per subslice shown
    - Sampler, supporting both media and 3D functions
    - Gateway (GWY)
    - Instruction cache (IC)
    - Local Thread Dispatcher (TDL)
    - Barycentric Calculator (BC)
    - Pixel Shader Dispatcher (PSD)
    - Data Cluster (HDC)
    - Dataport Render Cache (DAPRC) - two per subslice
- Slice Common – Scalable fixed function assets which support the compute horsepower provided two or more subslices.
    - 3D Fixed Function:
        - Windower/Mask unit (WM)
        - Plane-Z, Hi-Z (HZ) and Intermediate Z (IZ)
        - Setup Backend (SBE)
        - Pixel backend units
        - 3D stream caches for color, multi-sample surface, iz, and stencil (RCC$, MSC$, HZ$, RCZ$, STC$)
    - Media Fixed Function:
        - DAPRSC
        - RCPFE, BE
        - SVL
        - TDC
- L3 Cache – backing L3 cache for certain memory streams emanating from subslices.
    - L3 Data cache with support for data, URB, and shared local memory (SLM)

Device Attributes

Product Configuration Attribute Table		
Product Family	**CHV / BSW**	
Architectural Name	**2x6**	**2x8**
Slice count	1	1
Subslice Count	2	2
EU/Subslice	6	8
EU count (total)	12	16
Thread Count	7	7
Thread Count (Total)	84	112
FLOPs/Clk - Half Precision, MAD (peak)	384	512
FLOPs/Clk - Single Precision, MAD (peak)	192	256
FLOPs/Clk - Double Precision, MAD (peak)	24	32
Unslice clocking (coupled/decoupled from Cr slice)	coupled	coupled
GTI / Ring Interfaces	1	1
GTI bandwidth (bytes/unslice-clk)	64: R	64: R
	64: W	64: W
L3 Cache, total size (bytes)	384K	384K
L3 Cache, bank count	2	2
L3 Cache, bandwidth (bytes/clk)		
L3 Cache, D$ Size (Kbytes)	192K-256K	192K-256K
URB Size (kbytes)	64K-192K	64K-192K
SLM Size (kbytes)	0, 128K	0, 128K
LLC/L4 size (bytes)	N/A	N/A
Instruction Cache (IC, bytes)	2x 48K	2x 48K
Color Cache (RCC, bytes)	24K	24K
MSC Cache (MSC, bytes)	12K	12K
HiZ Cache (HZC, bytes)	8K	8K
Z Cache (RCZ, bytes)	16K	16K
Stencil Cache (STC, bytes)	4K	4K
L1 Texture Cache (bytes)	2x 32K	2x 32K
MT Texture Cache (bytes)	2x 8K	2x 8K
FMAD, SP (ops/EU/clk)	8	8
FMUL, SP (ops/EU/clk)	8	8
FADD, SP (ops/EU/clk)	8	8
MIN,MAX, SP (ops/EU/clk)	8	8
CMP, SP (ops/EU/clk)	8	8

Configurations

Product Configuration Attribute Table		
INV, SP (ops/EU/clk)	2	2
SQRT, SP (ops/EU/clk)	2	2
RSQRT, SP (ops/EU/clk)	2	2
LOG, SP (ops/EU/clk)	2	2
EXP, SP (ops/EU/clk)	2	2
POW, SP (ops/EU/clk)	1	1
IDIV, SP (ops/EU/clk)	1-6	1-6
TRIG, SP (ops/EU/clk)	2	2
FDIV, SP (ops/EU/clk)	1	1
Data Ports (HDC)	2	2
L3 Load/Store - same addresses within msg (dwords/clk)	2x 32	2x 32
L3 Load/Store - unique addresses within msg (dwords/clk)		
SLM Load//Store - same addresses within msg (dwords/clk)		
SLM Load//Store - unique addresses within msg (dwords/clk)		
Atomic, Local 32b - same addresses within msg (dwords/clk)	2x 16	2x 16
Atomic, Global 32b - unique addresses within msg (dwords/clk)	2x 16	2x 16
Geometry pipes	1	1
Samplers (3D)	2	2
Texel Rate, point, 32b (tex/clk)	8	8
Texel Rate, point, 64b (tex/clk)	8	8
Texel Rate, point, 128b (tex/clk)	8	8
Texel Rate, bilinear, 32b (tex/clk)	8	8
Texel Rate, bilinear, 64b (tex/clk)	8	8
Texel Rate, bilinear, 128b (tex/clk)	2	2
Texel Rate, trilinear, 32b (tex/clk)	4	4
Texel Rate, trilinear, 64b (tex/clk)	2	2
Texel Rate, trilinear, 128b (tex/clk)	1	1
Texel Rate, aniso 2x, 32b (tex/clk)	2	2
Texel Rate, aniso 4x, 32b (tex/clk)	1	1
Texel Rate, ansio 8x, 32b (tex/clk)	0.5	0.5
Texel Rate, ansio 16x, 32b (tex/clk)	0.25	0.25
HiZ Rate, (ppc)	32	32
IZ Rate, (ppc)	16	16
Stencil Rate (ppc)	32	32
(500 MHz, DDR-1600 or eDRAM; Range depends on dynamic compression ratio)		
Pixel Rate, fill, 32bpp (pix/clk, RCC hit)	4	4

Product Configuration Attribute Table		
Pixel Rate, fill, 32bpp (pix/clk, LLC hit @ 1.0x unslice clk)	N/A	N/A
Pixel Rate, fill, 32bpp (pix/clk, LLC hit, @ 1.5x unslice clk)	N/A	N/A
Pixel Rate, fill, 32bpp (pix/clk, memory, @ 1.0x unslice clk)	4	4
Pixel Rate, fill, 32bpp (pix/clk, memory, @ 1.5x unslice clk)	N/A	N/A
(500 MHz, DDR-1600 or eDRAM; Range depends on dynamic compression ratio)		
Pixel Rate, blend, 32bpp (p/clk, RCC hit)	4	4
Pixel Rate, blend, 32bpp (p/clk, LLC hit, @ 1.0x unslice clk)	N/A	N/A
Pixel Rate, blend, 32bpp (p/clk, LLC hit, @ 1.5x unslice clk)	N/A	N/A
Pixel Rate, blend, 32bpp (pix/clk, memory, @ 1.0x unslice clk)	4	4
Pixel Rate, blend, 32bpp (pix/clk, memory, @ 1.5x unslice clk)	N/A	N/A
Samplers (media)	2	2
VDBox Instances	1	1
VEBox Instances	1	1
SFC Instances	N/A	N/A
WGBox Instances	N/A	N/A

Programming Note	
Context:	Device Attributes
Unslice clock and slice clock are coupled; independent frequency control is not supported.	

Steppings and Device IDs

GT SKUs and Device IDs: The following table lists current GT Die / Packages for Cherry Trail (CHT) and Braswell (BSW).

Program Name	Gen	GT SKU	Total EUs	CPU / GT Stepping	GT Device2 Native ID	GT Device2 Revision ID	Comments / Description
CHT	Gen8LP	2x6	12	C0	0x22B0	0x20, 0x22, or 0x23 (depending on packaging)	Production Devices: Atom x5 series
CHT	Gen8LP	2x8	16	C0	0x22B0	0x20, 0x22, or 0x23 (depending on packaging)	Production Devices: Atom x7 series
BSW	Gen8LP	2x6	12	C0	0x22B1	0x21	Production Devices: Celeron QC and and Celeron DC series
BSW	Gen8LP	2x8	16	C0	0x22B1	0x21	Production Devices: Pentium QC series

Programming Note	
Project:	CHV
Context:	Steppings and Device IDs
See the DID [CHV] register.	