Intel® UHD Graphics Open Source

Programmer's Reference Manual

For the 2019 - 2020 Intel Core™ Processors, Pentium® Gold Processors, and Celeron® Processors based on the "Comet Lake" Platform

Volume 1: Configurations

April 2020, Revision 1.0

Creative Commons License

You are free to Share - to copy, distribute, display, and perform the work under the following conditions:

- **Attribution.** You must attribute the work in the manner specified by the author or licensor (but not in any way that suggests that they endorse you or your use of the work).
- **No Derivative Works.** You may not alter, transform, or build upon this work.

Notices and Disclaimers

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

A "Mission Critical Application" is any application in which failure of the Intel Product could result, directly or indirectly, in personal injury or death. SHOULD YOU PURCHASE OR USE INTEL'S PRODUCTS FOR ANY SUCH MISSION CRITICAL APPLICATION, YOU SHALL INDEMNIFY AND HOLD INTEL AND ITS SUBSIDIARIES, SUBCONTRACTORS AND AFFILIATES, AND THE DIRECTORS, OFFICERS, AND EMPLOYEES OF EACH, HARMLESS AGAINST ALL CLAIMS COSTS, DAMAGES, AND EXPENSES AND REASONABLE ATTORNEYS' FEES ARISING OUT OF, DIRECTLY OR INDIRECTLY, ANY CLAIM OF PRODUCT LIABILITY, PERSONAL INJURY, OR DEATH ARISING IN ANY WAY OUT OF SUCH MISSION CRITICAL APPLICATION, WHETHER OR NOT INTEL OR ITS SUBCONTRACTOR WAS NEGLIGENT IN THE DESIGN, MANUFACTURE, OR WARNING OF THE INTEL PRODUCT OR ANY OF ITS PARTS.

Intel may make changes to specifications and product descriptions at any time, without notice. Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined". Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. The information here is subject to change without notice. Do not finalize a design with this information.

The products described in this document may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Implementations of the I2C bus/protocol may require licenses from various entities, including Philips Electronics N.V. and North American Philips Corporation.

Intel and the Intel logo are trademarks of Intel Corporation in the U.S. and other countries.

* Other names and brands may be claimed as the property of others.

Table of Contents

Configurations Overview

The Intel Graphics Architecture was first introduced to the market in 2004. Since that time, the architecture and implementation have evolved to add many new features, increase performance, and improve power efficiency.

Each product generation has its own configurations chapter. Each chapter has a section for each project, and each project contains the following subsections:

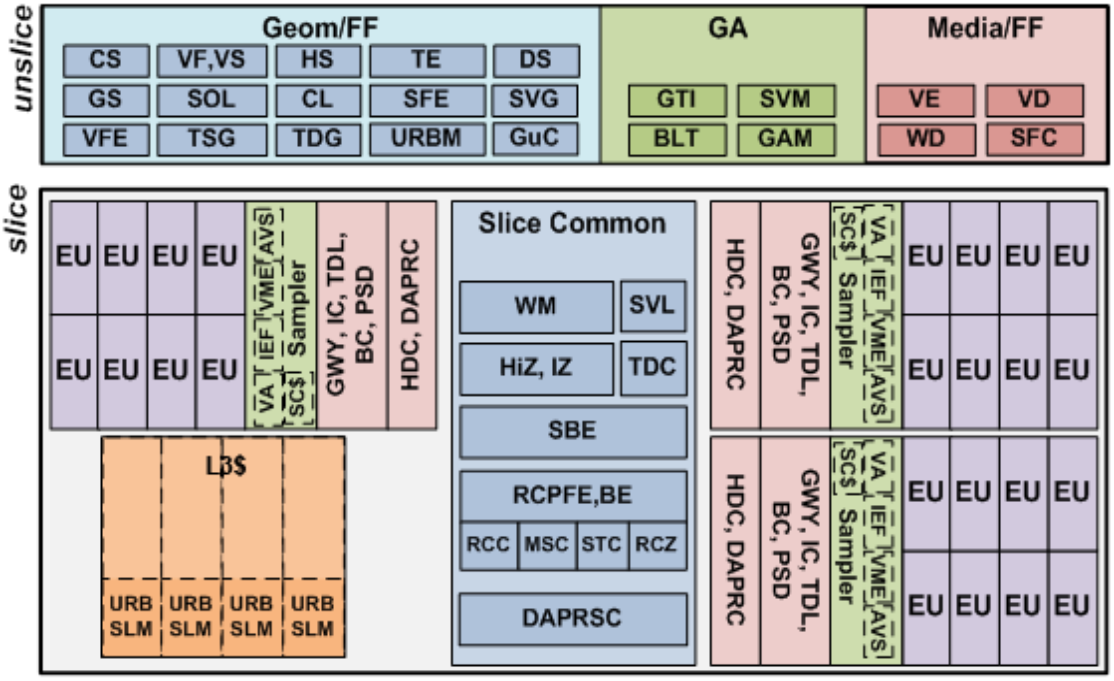
- Top Level Block Diagrams - Shows basic feature blocks of the project's graphics architecture for GT configurations.
- Device Attributes - Lists details of the graphics configuration options for each project.
- Steppings and Device IDs - Lists all the current unique GT Die / Packages for a specific project.

Top Level Block Diagrams CML

The diagrams below show basic feature blocks of the Comet Lake (CML) graphics architecture.

GT2 Configuration

The GT2 configuration contains one Unslice and one Slice with separate power domains for each, although they share a single clock domain.



This diagram is based on the following functional partitions:

(a) Geometry Fixed Functions (Geom/FF)

(b) Media Fixed Functions (Media/FF)

(c) Global Assets and GT Interface (GA)

(d) One or more Subslices (three shown)

(e) A Slice Common block

(f) An L3 Cache (L3$) block

Note that the combination of (a), (b), and (c) is typically referred to as the “unslice”, while a combination of (d), (e), and (f) is referred to as a compute “slice”.

The functionality in each of these groupings is further broken down as follows:

- Unslice – Fixed function pipelines for 3D, GPGPU, and Media operations, and interface to the outside world.

    - The 3D Geometry / Fixed Function (Geom/FF) block consisting of:
        - 3D fixed function pipeline (CS, VFVS, HS, TE, DS, GS, SOL, SL, SFE, SVG)
        - Video Front-End unit (VFE)
        - Thread Spawner unit (TSG) and the global Thread Dispatcher unit (TDG)
        - Unified Return Buffer Manager (URBM)

    - Media fixed function assets:
        - Video Decode (VD) Box
        - Video Encode (VE) Box
        - Wireless Display (WD) BOX
        - Scaler & Format Converter (SFC)
    - The Global Assets (GA) block as the primary interface and memory stream gateway to the outside world, consisting of:
        - GT Interface (GTI)
        - State Variable Manager (SVM)
        - Blitter (BLT)
        - Graphics Arbiter (GAM)
- Subslice (three shown) – A compute unit with supporting fixed- or shared-function assets sufficient for the EU capability.
    - A bank of Execution Units (EUs) – eight per subslice shown
    - Sampler, supporting both media and 3D functions
    - Gateway (GWY)
    - Instruction cache (IC)
    - Local Thread Dispatcher (TDL)
    - Barycentric Calculator (BC)
    - Pixel Shader Dispatcher (PSD)
    - Data Cluster (HDC)
    - Dataport Render Cache (DAPRC) - two per subslice
- Slice Common – Scalable fixed function assets which support the compute horsepower provided two or more subslices.
    - 3D Fixed Function:
        - Windower/Mask unit (WM)
        - Hi-Z (HZ) and Intermediate Z (IZ)
        - Setup Backend (SBE)
        - RCPFE, BE
        - 3D stream caches (RCC, MSC, STC, RCZ)

    - Media Fixed Functions:
        - DAPRSC
        - SVL
        - TDC
- L3 Cache – backing L3 cache for certain memory streams emanating from subslices.
    - L3 Data cache with support for data, URB, and shared local memory (SLM)

Device Attributes CML

The following table lists detailed GT device attributes for proposed Comet Lake (CML) SKUs.

NOTE: This information is preliminary, and subject to change.

Product Configuration Attribute Table		
Product Family	**CML**	
Architectural Name *	**1x2x6**	**1x3x8**
SKU Name	**GT1F**	**GT2**
Global Attributes		
Slice count	1	1
Subslice Count	2	3
EU/Subslice	6	8
EU count (total)	12	23 / 24 [b]
Thread Count	7	7
Thread Count (Total)	84	161 / 168
FLOPs/Clk - Half Precision, MAD (peak)	384	736 / 768
FLOPs/Clk - Single Precision, MAD (peak)	192	368 / 384
FLOPs/Clk - Double Precision, MAD (peak)	48	92 / 96
Unslice clocking (coupled/decoupled from Cr slice)	coupled	coupled
GTI / Ring Interfaces	1	1
GTI bandwidth (bytes/unslice-clk)	64: R	64: R
	64: W	64: W
eDRAM Support	N/A	N/A
Graphics Virtual Address Range	48 bit	48 bit
Graphics Physical Address Range	39 bit	39 bit
Caches & Dedicated Memories		
L3 Cache, total size (bytes)	384K	768K
L3 Cache, bank count	2	4
L3 Cache, bandwidth (bytes/clk)	2x 64: R 2x 64: W	4x 64: R 4x 64: W
L3 Cache, D$ Size (Kbytes)	192K - 256K	512K
URB Size (kbytes)	128K - 192K	384K
SLM Size (kbytes)	0, 128K	0, 192K
LLC/L4 size (bytes) [1]	~2MB/CPU core	~2MB/CPU core

Product Configuration Attribute Table		
Instruction Cache (IC, bytes)	2x 48K	3x 48K
Color Cache (RCC, bytes)	24K	24K
MSC Cache (MSC, bytes)	16K	16K
HiZ Cache (HZC, bytes)	12K	12K
Z Cache (RCZ, bytes)	32K	32K
Stencil Cache (STC, bytes)	8K	8K
Instruction Issue Rates		
FMAD, SP (ops/EU/clk)	8	8
FMUL, SP (ops/EU/clk)	8	8
FADD, SP (ops/EU/clk)	8	8
MIN,MAX, SP (ops/EU/clk)	8	8
CMP, SP (ops/EU/clk)	8	8
INV, SP (ops/EU/clk)	2	2
SQRT, SP (ops/EU/clk)	2	2
RSQRT, SP (ops/EU/clk)	2	2
LOG, SP (ops/EU/clk)	2	2
EXP, SP (ops/EU/clk)	2	2
POW, SP (ops/EU/clk)	1	1
IDIV, SP (ops/EU/clk)	1-6	1-6
TRIG, SP (ops/EU/clk)	2	2
FDIV, SP (ops/EU/clk)	1	1
Load/Store		
Data Ports (HDC)	2	3
L3 Load/Store (dwords/clk)	2x 64	3x 64
SLM Load/Store (dwords/clk)	2x 64	3x 64
Atomic Inc, 32b - sequential addresses (dwords/clk)	2x 64	3x 64
Atomic Inc, 32b - same address (dwords/clk)	2x 4	3x 4
Atomic CmpWr, 32b - sequential addresses (dwords/clk)	2x 32	3x 32
Atomic CmpWr, 32b - same address (dwords/clk)	2x 4	3x 4
3D Attributes		
Geometry pipes	1	1
Samplers (3D)	2	3
Texel Rate, point, 32b (tex/clk)	8	12

Product Configuration Attribute Table		
Texel Rate, point, 64b (tex/clk)	8	12
Texel Rate, point, 128b (tex/clk)	8	12
Texel Rate, bilinear, 32b (tex/clk)	8	12
Texel Rate, bilinear, 64b (tex/clk)	8	12
Texel Rate, bilinear, 128b (tex/clk)	2	3
Texel Rate, trilinear, 32b (tex/clk)	8	12
Texel Rate, trilinear, 64b (tex/clk)	4	6
Texel Rate, trilinear, 128b (tex/clk)	1	1.5
Texel Rate, aniso 2x, MIP Linear,, 32b (tex/clk)	2	3
Texel Rate, aniso 4x, MIP Linear,, 32b (tex/clk)	1	1.5
Texel Rate, aniso 8x, MIP Linear,, 32b (tex/clk)	0.5	0.75
Texel Rate, aniso 16x, MIP Linear,, 32b (tex/clk)	0.25	0.375
HiZ Rate, (ppc)	64	64
IZ Rate, (ppc)	16	16
Stencil Rate (ppc)	64	64
(500 MHz, DDR-2400 or eDRAM; Range depends on dynamic compression ratio)		
Pixel Rate, fill, 32bpp (pix/clk, RCC hit)	8	8
Pixel Rate, fill, 32bpp (pix/clk, LLC hit @ 1.0x unslice clk) [2]		
Pixel Rate, fill, 32bpp (pix/clk, LLC hit, @ 1.5x unslice clk) [2]	N/A	N/A
Pixel Rate, fill, 32bpp (pix/clk, memory, @ 1.0x unslice clk) [2]		
Pixel Rate, fill, 32bpp (pix/clk, memory, @ 1.5x unslice clk) [2]	N/A	N/A
(500 MHz, DDR-2400 or eDRAM; Range depends on dynamic compression ratio)		
Pixel Rate, blend, 32bpp (p/clk, RCC hit)	8	8
Pixel Rate, blend, 32bpp (p/clk, LLC hit, @ 1.0x unslice clk) [2]		

Product Configuration Attribute Table		
Pixel Rate, blend, 32bpp (p/clk, LLC hit, @ 1.5x unslice clk) [2]	N/A	N/A
Pixel Rate, blend, 32bpp (pix/clk, memory, @ 1.0x unslice clk) [2]		
Pixel Rate, blend, 32bpp (pix/clk, memory, @ 1.5x unslice clk) [2]	N/A	N/A
Media Attributes		
Samplers (media)	2	3
VDBox Instances	1	1
VEBox Instances	1	1
SFC Instances	1	1
WGBox Instances	N/A	N/A
Display Attributes		
Display Pipes	3	3
Display Planes per Pipe	3	3
DDI ports	2	2
eDP ports	1	1

Footnotes:

* Architectural Name = Slice Count x Subslice Count x EUs per Subslice

[a] SKU naming & details has not yet been decided.

[b] One EU reserved for die recovery purposes.

Stepping and Device IDs CML

The following table lists currently proposed variations of GT Die / Packages for Comet Lake (CML).

This information is preliminary, and subject to change at any time.

Segment	SKU	TDP	EUs	CPU Brand	Brand #	GFX Name	CPU Stepping	GT/Display Version	DID2 Grouping	DID2	Rev ID
Mobile	U42	15	24	Cor i7/i5	N/A	Intel® UHD Graphics	WHL V0	CFL C0 / KBL C0	1	0x9B41	0x2
Mobile	U2f2	15	23	Core i3	N/A	Intel® UHD Graphics	WHL V0	CFL C0 / KBL C0	1	0x9B41	0x2
Mobile	U2f1f	15	12	Pentium/Celeron	N/A	Intel® UHD Graphics	WHL V0	CFL C0 / KBL C0	2	0x9B21	0x2
Mobile	U62	15	24	Core i7	N/A	Intel® UHD Graphics	CML A0	CFL E0 / KBL C0	3	0x9BCA	0x4
Mobile	U4f2	15	24	Core i7/i5	N/A	Intel® UHD Graphics	CML A0	CFL E0 / KBL C0	3	0x9BCA	0x4
Mobile	U2f2	15	23	Core i3	N/A	Intel® UHD Graphics	CML A0	CFL E0 / KBL C0	3	0x9BCA	0x4
Mobile	U2f1f	15	12	Pentium/ Celeron	N/A	Intel® UHD Graphics	CML A0	CFL E0 / KBL C0	4	0x9BAA	0x4
Mobile	U62	15	24	Core i7	N/A	Intel® UHD Graphics	CML K0	CFL F0 / KBL C0	7	0x9BCC	0x5
Mobile	U4f2	15	24	Core i7/i5	N/A	Intel® UHD Graphics	CML K0	CFL F0 / KBL C0	7	0x9BCC	0x5
Mobile	U2f2	15	23	Core i3	N/A	Intel® UHD Graphics	CML K0	CFL F0 / KBL C0	7	0x9BCC	0x5
Mobile	U2f1f	15	12	Pentium/ Celeron	N/A	Intel® UHD Graphics	CML K0	CFL F0 / KBL C0	8	0x9BAC	0x5
Desktop	S10+2	35/65/95	24	Core i9	630	Intel® UHD Graphics	CML P0	CFL F0 / KBL C0	11	0x9BC5	0x5
Desktop	S8f2	35/65/95	24	Core i7	630	Intel® UHD Graphics	CML P0	CFL F0 / KBL C0	11	0x9BC5	0x5
Desktop	S6f2	35/65/95	24	Core i5	630	Intel® UHD Graphics	CML P0	CFL F0 / KBL C0	11	0x9BC5	0x5
Desktop	S62	35/65/95	24	Core i5	630	Intel® UHD Graphics	CML G0	CFL E0 / KBL C0	13	0x9BC8	0x4
Desktop	S4f2	35/65/95	24	Core i3	630	Intel® UHD Graphics	CML G0	CFL E0 / KBL C0	13	0x9BC8	0x4
Desktop	S2f2	35/65/95	24	Pentium	630	Intel® UHD Graphics	CML G0	CFL E0 / KBL C0	13	0x9BC8	0x4
Desktop	S2f1f	35/65/95	12	Pentium & Celeron	610	Intel® UHD Graphics	CML G0	CFL E0 / KBL C0	14	0x9BA8	0x4
Mobile	H82	45/65	24	Core i9	N/A	Intel® UHD Graphics	R2	CFL F0 / KBL C0	15	0x9BC4	0x5

Segment	SKU	TDP	EUs	CPU Brand	Brand #	GFX Name	CPU Stepping	GT/Display Version	DID2 Grouping	DID2	Rev ID
Mobile	H6f2	45	24	Core i7	N/A	Intel® UHD Graphics	R2	CFL F0 / KBL C0	15	0x9BC4	0x5
Mobile	H4f2	45	24/23	Core i5	N/A	Intel® UHD Graphics	R2	CFL F0 / KBL C0	15	0x9BC4	0x5
Mobile	H81	45	12	Core i9	N/A	Intel® UHD Graphics	R2	CFL F0 / KBL C0	16	0x9BA4	0x5
Mobile	H6f1f	45	12	Core i7	N/A	Intel® UHD Graphics	R2	CFL F0 / KBL C0	16	0x9BA4	0x5
Mobile Xeon	H82	45	24	Xeon W	P630	Intel® UHD Graphics	R2	CFL F0 / KBL C0	15	0x9BF6	0x5
Workstation	S10+2	125/ 80/35	24	Xeon W	P630	Intel® UHD Graphics	CML P0	CFL F0 / KBL C0	11	0x9BC6	0x5
Workstation	S62	80	24	Xeon W	P630	Intel® UHD Graphics	CML G0	CFL E0 / KBL C0	13	0x9BE6	0x4