Intel® Open Source HD Graphics and Intel Iris™ Graphics

Programmer's Reference Manual

For the 2014-2015 Intel Core™ Processors, Celeron™ Processors and Pentium™ Processors based on the "Broadwell" Platform

Volume 4: Configurations

November 2015, Revision 1.2

Creative Commons License

Notices and Disclaimers

Table of Contents

Configurations Overview

The Intel "Gen" Graphics Architecture was first introduced to the market in 2004. Since that time, the architecture and its implementation have evolved to add many new features, increase performance, and improve power efficiency.

This chapter contains configurations details for Broadwell (BDW) as described in the following sections:

- Top Level Block Diagrams
- Device Attributes
- Steppings and Device IDs

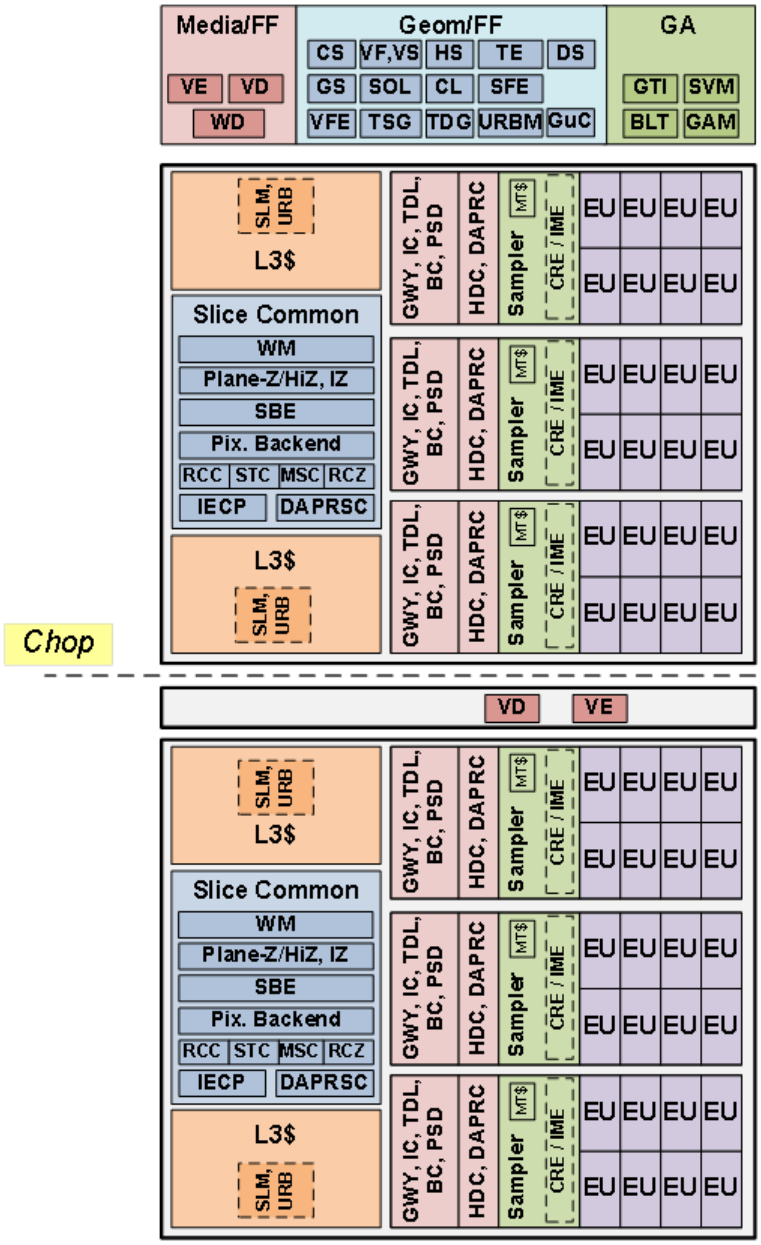
Configurations

This chapter contains configurations details as described in the following sections:

- Top Level Block Diagrams
- Device Attributes
- Steppings and Device IDs

Top Level Block Diagrams

The following diagram shows basic feature blocks of the Broadwell (BDW) graphics architecture arranged in a GT3 configuration, with the portion above the "Chop" line representing the GT2 configuration:



This diagram is based on the following functional partitions:

(a) Geometry Fixed Functions

(b) Media Fixed Functions

(c) Global Assets and GT Interface

(d) One or more Subslices (three shown)

(e) A Slice-Common block

(f) An L3 Cache (L3$) block

Note that the combination of (a), (b), and (c) is typically referred to as the "unslice", while a combination of (d), (e), and (f) is referred to as a compute "slice".

The functionality in each of these groupings is further broken down as follows:

- Unslice – Fixed function pipelines for 3D, GPGPU, and Media operations, and interface to the outside world.
  - The 3D Geometry / Fixed Function (Geom/FF) block consisting of:
    - 3D fixed function pipeline (CS, VFVS, HS, TE, DS, GS, SOL, SL, SFE)
    - Video Front-End unit (VFE)
    - Thread Spawner unit (TSG) and the global Thread Dispatcher unit (TDG)
    - Unified Return Buffer Manager (URBM)
  - Media fixed function assets:
    - Video Decode (VD) Box
    - Video Encode (VE) Box
    - Wireless Display (WD) BOX
  - The Global Assets (GA) block as the primary interface and memory stream gateway to the outside world, consisting of:
    - GT Interface (GTI)
    - State Variable Manager (SVM)
    - Blitter (BLT)
    - Graphics Arbiter (GAM)
- Subslice (three shown) – A compute unit with supporting fixed- or shared-function assets sufficient for the EU capability.
  - A bank of Execution Units (EUs) – eight per subslice shown
  - Sampler, supporting both media and 3D functions
  - Gateway (GWY)
  - Instruction cache (IC)
  - Local Thread Dispatcher (TDL)
  - Barycentric Calculator (BC)
  - Pixel Shader Dispatcher (PSD)

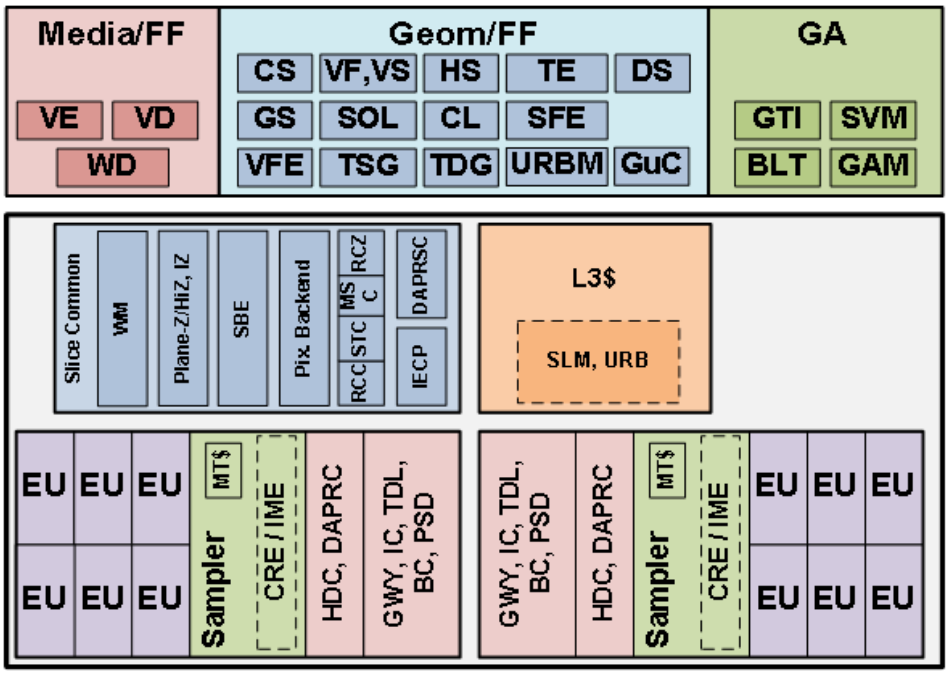
    - Data Cluster (HDC)
    - Dataport Render Cache (DAPRC)
- Slice Common – Scalable fixed function assets which support the compute horsepower provided two or more subslices.
    - 3D Fixed Function:
        - Windower/Mask unit (WM)
        - Plane-Z, Hi-Z (HZ) and Intermediate Z (IZ)
        - Setup Backend (SBE)
        - Pixel backend units
        - 3D stream caches for color, multi-sample surface, iz, and stencil (RCC, MSC, RCZ, STC)
    - Media Fixed Function:
        - DAPRSC
- L3 Cache – backing L3 cache for certain memory streams emanating from subslices.
    - L3 Data cache with support for data, URB, and shared local memory (SLM)

Slices and unslices are combined to create three product configurations:

- GT3: A single unslice coupled with two slices, plus an added VD and VE unit (see above)
- GT2: A single unslice coupled with a single slice (see above)
- GT1: The smallest configuration uses a reduced unslice and a reduced slice (see below)

GT1 Configuration

The GT1 configuration is an opportunistic reduction of GT2, as shown in the following diagram:



Device Attributes

Product Configuration Attribute Table						
Product Family	**BDW**					
Architectural Name	**1x2x6**	**1x3x6**	**1x3x8**	**1x3x8**	**2x6x8**	**2x6x8**
SKU Name	**GT1F**	**GT1.5F**	**GT2F**	**GT2**	**GT3F**	**GT3**
Global Attributes						
Slice count	1	1	1	1	2	2
Subslice Count	2	3	3	3	6	6
EU/Subslice	6	6	8	8	8	8
EU count (total)	12	18	23 [a]	24	47 [a]	48
Thread Count	7	7	7	7	7	7
Thread Count (Total)	84	126	161	168	329	336
FLOPs/Clk - Half Precision, MAD (peak)	384	576	736	768	1504	1536
FLOPs/Clk - Single Precision, MAD (peak)	192	288	368	384	752	768
FLOPs/Clk - Double Precision, MAD (peak)	48	72	92	96	188	192
Unslice clocking (coupled/decoupled from Cr slice)	coupled	coupled	coupled	coupled	coupled	coupled
GTI / Ring Interfaces	1	1	1	1	1	1
GTI bandwidth (bytes/unslice-clk)	64: R	64: R	64: R	64: R	64: R	64: R
	32: W	32: W	32: W	32: W	64: W	64: W
eDRAM Support	N/A	N/A	N/A	N/A	N/A	0, 128MB
Caches & Dedicated Memories						
L3 Cache, total size (bytes)	384K	768K	768K	768K	1.5M	1.5M
L3 Cache, bank count	2	4	4	4	8	8
L3 Cache, bandwidth (bytes/clk)	2x 64: R 2x 64: W	4x 64: R 4x 64: W	4x 64: R 4x 64: W	4x 64: R 4x 64: W	8x 64: R 8x 64: W	8x 64: R 8x 64: W
L3 Cache, D$ Size (Kbytes)	192K-320K	384K-576K	384K-576K	384K-576K	768K-1024K	768K-1024K
URB Size (kbytes)	64K-192K	128K-384K	128K-384K	128K-384K	256K-768K	256K-768K
SLM Size (kbytes)	0, 128K	0, 192K	0, 192K	0, 192K	0, 384K	0, 384K
LLC/L4 size (bytes)	~2MB/CPU core	~2MB/CPU core	~2MB/CPU core	~2MB/CPU core	~2MB/CPU core	~2MB/CPU core
Instruction Cache (IC, bytes)	2x 48K	3x 48K	3x 48K	3x 48K	6x 48K	6x 48K
Color Cache (RCC, bytes)	24K	24K	24K	24K	2x 24K	2x 24K
MSC Cache (MSC, bytes)	12K	12K	12K	12K	2x 12K	2x 12K

Product Configuration Attribute Table						
HiZ Cache (HZC, bytes)	12K	12K	12K	12K	2x 12K	2x 12K
Z Cache (RCZ, bytes)	32K	32K	32K	32K	2x 12K	2x 12K
Stencil Cache (STC, bytes)	8K	8K	8K	8K	2x 8K	2x 8K
L1 Texture Cache (bytes)	2x 32K	3x 32K	3x 32K	3x 32K	6x 32K	6x 32K
MT Texture Cache (bytes)	2x 8K	3x 8K	3x 8K	3x 8K	6x 8K	6x 8K
Instruction Issue Rates						
FMAD, SP (ops/EU/clk)	8	8	8	8	8	8
FMUL, SP (ops/EU/clk)	8	8	8	8	8	8
FADD, SP (ops/EU/clk)	8	8	8	8	8	8
MIN,MAX, SP (ops/EU/clk)	8	8	8	8	8	8
CMP, SP (ops/EU/clk)	8	8	8	8	8	8
INV, SP (ops/EU/clk)	2	2	2	2	2	2
SQRT, SP (ops/EU/clk)	2	2	2	2	2	2
RSQRT, SP (ops/EU/clk)	2	2	2	2	2	2
LOG, SP (ops/EU/clk)	2	2	2	2	2	2
EXP, SP (ops/EU/clk)	2	2	2	2	2	2
POW, SP (ops/EU/clk)	1	1	1	1	1	1
IDIV, SP (ops/EU/clk)	1-6	1-6	1-6	1-6	1-6	1-6
TRIG, SP (ops/EU/clk)	2	2	2	2	2	2
FDIV, SP (ops/EU/clk)	1	1	1	1	1	1
Load/Store						
Data Ports (HDC)	2	3	3	3	6	6
L3 Load/Store (bytes/clk)	2x 64	3x 64	3x 64	3x 64	6x 64	6x 64
SLM Load/Store (bytes/clk)	2x 64	3x 64	3x 64	3x 64	6x 64	6x 64
Atomic Inc, 32b - sequential addresses (bytes/clk)	2x 64	3x 64	3x 64	3x 64	6x 64	6x 64
Atomic Inc, 32b - same address (bytes/clk)	2x 4	3x 4	3x 4	3x 4	6x 4	6x 4
Atomic CmpWr, 32b - sequential addresses (bytes/clk)	2x 32	3x 32	3x 32	3x 32	6x 32	6x 32
Atomic CmpWr, 32b - same address (bytes/clk)	2x 4	3x 4	3x 4	3x 4	6x 4	6x 4
3D Attributes						
Geometry pipes	1	1	1	1	1	1
Samplers (3D)	2	3	3	3	6	6
Texel Rate, point, 32b (tex/clk)	8	12	12	12	24	24
Texel Rate, point, 64b (tex/clk)	8	12	12	12	24	24
Texel Rate, point, 128b (tex/clk)	8	12	12	12	24	24

Product Configuration Attribute Table						
Texel Rate, bilinear, 32b (tex/clk)	8	12	12	12	24	24
Texel Rate, bilinear, 64b (tex/clk)	8	12	12	12	24	24
Texel Rate, bilinear, 128b (tex/clk)	2	3	3	3	6	6
Texel Rate, trilinear, 32b (tex/clk)	4	6	6	6	12	12
Texel Rate, trilinear, 64b (tex/clk)	2	3	3	3	6	6
Texel Rate, trilinear, 128b (tex/clk)	1	1.5	1.5	1.5	3	3
Texel Rate, aniso 2x, 32b (tex/clk)	2	3	3	3	6	6
Texel Rate, aniso 4x, 32b (tex/clk)	1	1.5	1.5	1.5	3	3
Texel Rate, ansio 8x, 32b (tex/clk)	0.5	0.75	0.75	0.75	1.5	1.5
Texel Rate, ansio 16x, 32b (tex/clk)	0.25	0.375	0.375	0.375	0.75	0.75
HiZ Rate, (ppc)	64	64	64	64	2x 64	2x 64
IZ Rate, (ppc)	16	16	16	16	2x 16	2x 16
Stencil Rate (ppc)	64	64	64	64	2x 16	2x 64
(500 MHz, DDR-2400 or eDRAM; Range depends on dynamic compression ratio)						
Pixel Rate, fill, 32bpp (pix/clk, RCC hit)	4	6	6	6	12	12
Pixel Rate, fill, 32bpp (pix/clk, LLC hit @ 1.0x unslice clk)	4	6	6	6	12	12
Pixel Rate, fill, 32bpp (pix/clk, LLC hit, @ 1.5x unslice clk)	N/A	N/A	N/A	N/A	N/A	N/A
Pixel Rate, fill, 32bpp (pix/clk, memory, @ 1.0x unslice clk)	4	6	6	6	12	12
Pixel Rate, fill, 32bpp (pix/clk, memory, @ 1.5x unslice clk)	N/A	N/A	N/A	N/A	N/A	N/A
(500 MHz, DDR-2400 or eDRAM; Range depends on dynamic compression ratio)						
Pixel Rate, blend, 32bpp (p/clk, RCC hit)	4	4	4	4	8	8
Pixel Rate, blend, 32bpp (p/clk, LLC hit, @ 1.0x unslice clk)	4	4	4	4	8	8
Pixel Rate, blend, 32bpp (p/clk, LLC hit, @ 1.5x unslice clk)	N/A	N/A	N/A	N/A	N/A	N/A
Pixel Rate, blend, 32bpp (pix/clk, memory, @ 1.0x unslice clk)	4	4	4	4	8	8

Product Configuration Attribute Table						
Pixel Rate, blend, 32bpp (pix/clk, memory, @ 1.5x unslice clk)	N/A	N/A	N/A	N/A	N/A	N/A
Media Attributes						
Samplers (media)	2	3	3	3	6	6
VDBox Instances	1	1	1	1	2	2
VEBox Instances	1	1	1	1	2	2

Note: [a] One EU is fused for die recovery purposes.

A brief explanation of the listed SKUs is as follows:

- GT1F has one slice containing two subslices, with two (of eight) EUs fused out in each subslice for a total of 2 x 6 = 12 EUs.
- GT1.5F has one slice containing three subslices, with two (of eight) EUs fused out in each subslice for a total of 3 x 6 = 18 EUs.
- GT2F has one slice containing three subslices of eight EUs each, with one EU fused off for a total of 3 x 8 - 1 = 23 EUs.
- GT2 has one slice containing three subslices of eight EUs each, for a total of 3 x 8 = 24 EUs.
- GT3F has two slices containing three subslices of eight EUs each, with one EU fused off for a total of 2 x 3 x 8 -1 = 47 EUs.
- GT3 has two slices containing three subslices of eight EUs each, for a total of 2 x 3 x 8 = 48 EUs.

Steppings and Device IDs

Unique Devices: The following table lists all currently planned GT Die / Packages for Gen8 (BDW). Prior to manufacturing, this information is subject to change at any time.

CPU SKU	GT SKU	Total EUs	CPU Stepping	GT/Disp Stepping	Native Device2 ID	Device2 Revision ID	Comments
2+2 ULT / ULX	GT2	24	E1	G1	0x1616 (ULT) or 0x161E (ULX)	0x8	Production devices
2+1 U	GT1	12	F0	H0	0x1606	0x9	Production devices: HD Graphics
2+2 ULT / ULX	GT2	24	F0	H0	0x1616 (ULT) or 0x161E (ULX)	0x9	Production devices: HD Graphics 5300, 5500
2+3 ULT / ULX	GT3	48	F0	H0	0x1626 (15W) or 0x162B (28W)	0x9	Production devices: HD Graphics 6000, 6100
4+2 H	GT2	24	G0	J0	0x1612	0xA	Production devices: HD Graphics 5600
4+3e Halo	GT3e	48	G0	J0	0x1622	0xA	Production devices: Iris Pro Graphics 6200, P5700
4+3e Halo	GT3e	48	G0	J0	0x162A	0xA	Production devices: Iris Pro Graphics P6300

Device IDs

The following table lists valid Device2 (GT) IDs for BDW.

Device2 ID	Description	Comments / SKU String	Number of EUs
0x1606	U-Processor - GT1	Intel HD graphics	12
0x1612	H-Processor - GT2	Intel HD graphics 5600	24
0x1616	U-Processor - GT2	Intel HD graphics 5500	High End SKUs: 24 Low End SKUs: 23*
0x161E	Y-Processsor - GT2	Intel HD graphics 5300, 5500	24
0x1622	Halo H-Processor (EDRAM) - GT3e	Intel Iris Pro graphics 6200, P5700	48
0x1626	U-Processor - GT3 15W	Intel HD graphics 6000	47*
0x162B	U-Processor - GT3 28W	Intel Iris graphics 6100	48
0x162A	H-Processor (EDRAM) - GT3e Server	Intel Iris Pro graphics P6300	48

Notes:

(*) Intel reserves the right to increase the number of EUs on these SKUs.

- Intel Core i3 processors (ULT) will have 23 EUs, but could move to 24 EUs in the future.