Intel® Open Source HD Graphics and Intel Iris™ Graphics

Programmer's Reference Manual

For the 2014-2015 Intel Core™ Processors, Celeron™ Processors and Pentium™ Processors based on the "Broadwell" Platform

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GFX PCI Registers

Address Space	Address	Symbol	Name
PCI: 0/0/0	00050h	GGC_0_0_0_PCI	GMCH Graphics Control
PCI: 0/0/0	00054h	DEVEN_0_0_0_PCI	Device Enable
PCI: 0/0/0	000B0h	BDSM_0_0_0_PCI	Base Data of Stolen Memory
PCI: 0/0/0	000B4h	BGSM_0_0_0_PCI	Base of GTT Stolen Memory
PCI: 0/0/0	000E4h	CAPID0_A_0_0_0_PCI	Capabilities A
PCI: 0/0/0	000E8h	CAPID0_B_0_0_0_PCI	Capabilities B
PCI: 0/2/0	00000h	VID2_0_2_0_PCI	Vendor Identification
PCI: 0/2/0	00002h	DID2_0_2_0_PCI	Device Identification
PCI: 0/2/0	00004h	PCICMD_0_2_0_PCI	PCI Command
PCI: 0/2/0	00006h	PCISTS2_0_2_0_PCI	PCI Status
PCI: 0/2/0	00008h	RID2_0_2_0_PCI	Revision Identification
PCI: 0/2/0	00009h	CC_0_2_0_PCI	Class Code
PCI: 0/2/0	0000Ch	CLS_0_2_0_PCI	Cache Line Size
PCI: 0/2/0	0000Dh	MLT2_0_2_0_PCI	Master Latency Timer
PCI: 0/2/0	0000Eh	HDR2_0_2_0_PCI	Header Type
PCI: 0/2/0	00010h	GTTMMADR_0_2_0_PCI	Graphics Translation Table Memory Mapped Range Address
PCI: 0/2/0	00018h	GMADR_0_2_0_PCI	Graphics Memory Range Address
PCI: 0/2/0	00020h	IOBAR_0_2_0_PCI	I/O Base Address
PCI: 0/2/0	0002Ch	SVID2_0_2_0_PCI	Subsystem Vendor Identification
PCI: 0/2/0	0002Eh	SID2_0_2_0_PCI	Subsystem Identification
PCI: 0/2/0	00030h	ROMADR_0_2_0_PCI	Video BIOS ROM Base Address
PCI: 0/2/0	00034h	CAPPOINT_0_2_0_PCI	Capabilities Pointer
PCI: 0/2/0	0003Ch	INTRLINE_0_2_0_PCI	Interrupt Line
PCI: 0/2/0	0003Dh	INTRPIN_0_2_0_PCI	Interrupt Pin
PCI: 0/2/0	0003Eh	MINGNT_0_2_0_PCI	Minimum Grant
PCI: 0/2/0	0003Fh	MAXLAT_0_2_0_PCI	Maximum Latency
PCI: 0/2/0	00040h	CAPID0_0_2_0_PCI	Capability Identifier
PCI: 0/2/0	00042h	CAPCTRL0_0_2_0_PCI	Capabilities Control
PCI: 0/2/0	00044h	CAPID0_A_0_2_0_PCI	Mirror of Capabilities A
PCI: 0/2/0	00048h	CAPID0_B_0_2_0_PCI	Mirror of Capabilities B
PCI: 0/2/0	00050h	MGGC0_0_2_0_PCI	Mirror of GMCH Graphics Control
PCI: 0/2/0	00054h	DEVEN0_0_2_0_PCI	Mirror of Device Enable
PCI: 0/2/0	0005Ch	BDSM_0_2_0_PCI	Mirror of Base Data of Stolen Memory
PCI: 0/2/0	00060h	HSRW_0_2_0_PCI	Hardware Scratch Read Write

Address Space	Address	Symbol	Name
PCI: 0/2/0	00062h	MSAC_0_2_0_PCI	Multi Size Aperture Control
PCI: 0/2/0	00090h	MSI_CAPID_0_2_0_PCI	Message Signaled Interrupts Capability ID
PCI: 0/2/0	00092h	MC_0_2_0_PCI	Message Control
PCI: 0/2/0	00094h	MA_0_2_0_PCI	Message Address
PCI: 0/2/0	00098h	MD_0_2_0_PCI	Message Data
PCI: 0/2/0	000A4h	AFCIDNP_0_2_0_PCI	Advanced Features Capabilities Identifier and Next Pointer
PCI: 0/2/0	000A6h	AFLC_0_2_0_PCI	Advanced Features Length and Capabilities
PCI: 0/2/0	000A8h	AFCTL_0_2_0_PCI	Advanced Features Control
PCI: 0/2/0	000A9h	AFSTS_0_2_0_PCI	Advanced Features Status
PCI: 0/2/0	000D0h	Reserved	Reserved
PCI: 0/2/0	000D2h	Reserved	Reserved
PCI: 0/2/0	000D4h	Reserved	Reserved
PCI: 0/2/0	000E0h	SWSMI_0_2_0_PCI	Software SMI
PCI: 0/2/0	000E4h	GSE_0_2_0_PCI	Graphics System Event
PCI: 0/2/0	000E8h	SWSCI_0_2_0_PCI	Software SCI
PCI: 0/2/0	000FCh	ASLS_0_2_0_PCI	ASL Storage
PCI: 0/2/0	00100h	PASID_EXTCAP_0_2_0_PCI	PASID Extended Capability Header
PCI: 0/2/0	00104h	PASID_CAP_0_2_0_PCI	PASID Capability
PCI: 0/2/0	00106h	PASID_CTRL_0_2_0_PCI	PASID Control
PCI: 0/2/0	00200h	ATS_EXTCAP_0_2_0_PCI	ATS Extended Capability Header
PCI: 0/2/0	00204h	ATS_CAP_0_2_0_PCI	ATS Capability
PCI: 0/2/0	00206h	ATS_CTRL_0_2_0_PCI	ATS Control
PCI: 0/2/0	00300h	PR_EXTCAP_0_2_0_PCI	Page Request Extended Capability Header
PCI: 0/2/0	00304h	PR_CTRL_0_2_0_PCI	Page Request Control
PCI: 0/2/0	00306h	PR_STATUS_0_2_0_PCI	Page Request Status
PCI: 0/2/0	00308h	OPRC_0_2_0_PCI	Outstanding Page Request Capacity
PCI: 0/2/0	0030Ch	OPRA_0_2_0_PCI	Outstanding Page Request Allocation

GTTMMADR

MSA Registers

MPGFXTRK_CR_DPFC_CONTROL_SA_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x100100

Size: 32 bits

Access: RW

This register contains control bits related to Display Frame Buffer Compression Host Invalidation in System Agent.

Bit	Type	Default Value	RST Type	Description
29:29	RW	0x0	default/uncore/flr	**CPUFNCEN:** 0: Display Buffer is not in a CPU fence. No modifications are allowed from CPU to the Display Buffer. 1: Display Buffer exists in a CPU fence.
4:0	RW	0x0	default/uncore/flr	**CPUFNCNUM:** This field specifies the CPU visible FENCE number corresponding to the placement of the uncompressed frame buffer.

MPGFXTRK_CR_DPFC_CPU_FENCE_OFFSET_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x100104

Size: 32 bits

Access: RW

This register contains control bits related to Display Frame Buffer Compression Host Invalidation in System Agent.

Bit	Type	Default Value	RST Type	Description
21:0	RW	0x0	default/uncore/flr	**YFNCDISP:** Y offset from the CPU fence to the Display Buffer base

MPGFXTRK_CR_TILECTL_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x101000

Size: 32 bits

Access: RW

This register contains control functionality related to GFX Aperture Tiling.

Bit	Type	Default Value	RST Type	Description
3:3	RW	0x0	default/uncore/flr	**BKSNPDIS:** This bit allows to disable backsnoop requests as a result of IA requests to the Aperture. 0: Snoops are sent for IA requests that hit the Aperture 1: Snoops are never sent for IA requests that hit the Aperture
2:2	RW	0x0	default/uncore/flr	**DISTLBPF:** On Tile Y GFX TLB miss, the cacheline read from the GTT contains 16 PTEs. This bit indicates whether all 16 PTEs are required to be cached or only the PTE that was requested. 0 - Prefetch 15 entries into the GFX TLB in addition to the demand-based fetch for Tile Y 1 - Disable TLB prefetch for Tile Y
1:0	RW	0x0	default/uncore/flr	**SWZCTL:** This register location is updated via GFX Driver prior to enabling DRAM accesses. The Driver needs to obtain the need for memory address swizzling via DRAM configuration registers and set the following bits. 00b - No Address Swizzling 01b - Address bit 6 needs to be swizzled for tiled surfaces 10b - Reserved 11b - Reserved

MPGFXTRK_CR_GFX_FLSH_CNTL_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x101008

Size: 32 bits

Access: WO

This register is used to flush GFX TLBs in the System Agent.

Bit	Type	Default Value	RST Type	Description
0:0	WO	0x0	default/uncore	**GFX_FLSH_CNTL:** A CPU write to this bit flushes the GFX TLBs in the System Agent. The data associated with the write is discarded and a read returns all 0s.

MPGFXTRK_CR_MTOLUD_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x108000

Size: 32 bits

Access: RO_V

This 32 bit register defines the Top of Low Usable DRAM. TSEG, GTT Graphics memory and Graphics Stolen Memory are within the DRAM space defined. From the top, the Host optionally claims 1 to 64MBs of DRAM for internal graphics if enabled, 1or 2MB of DRAM for GTT Graphics Stolen Memory if enabled and 1, 2, or 8 MB of DRAM for TSEG if enabled.

Programming Example:

C1DRB3 is set to 4GB

TSEG is enabled and TSEG size is set to 1MB

Internal Graphics is enabled, and Graphics Mode Select is set to 32MB

GTT Graphics Stolen Memory Size set to 2MB

BIOS knows the OS requires 1G of PCI space.

BIOS also knows the range from 0FEC00000h to 0FFFFFFFFh is not usable by the system. This 20MB range at the very top of addressable memory space is lost to APIC and LT.

According to the above equation, TOLUD is originally calculated to: 4GB 100000000h

The system memory requirements are: 4GB max addressable space - 1GB pci space - 35MB lost memory 3GB - 35MB minimum granularity 0ECB00000h

Since 0ECB00000h PCI and other system requirements is less than 100000000h, TOLUD should be programmed to ECBh.

These bits are Intel TXT lockable.

Bit	Type	Default Value	RST Type	Description
31:20	RO_V	0x1	default/uncore	**TOLUD:** This register contains bits 31 to 20 of an address one byte above the maximum DRAM memory below 4G that is usable by the operating system. Address bits 31 down to 20 programmed to 01h implies a minimum memory size of 1MB. Configuration software must set this value to the smaller of the following 2 choices: maximum amount memory in the system minus ME stolen memory plus one byte or the minimum address allocated for PCI memory. Address bits 19:0 are assumed to be 00000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register. The Top of Low Usable DRAM is the lowest address above both Graphics Stolen memory and Tseg. BIOS determines the base of Graphics Stolen Memory by subtracting the Graphics Stolen Memory Size from TOLUD and further decrements by Tseg size to determine base of Tseg. This register must be 1MB aligned when reclaim is enabled.
0:0	RO_V	0x0	default/uncore	**LOCK:** This bit will lock all writeable settings in this register, including itself.

MPGFXTRK_CR_MGGC_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x108040

Size: 16 bits

Access: RO_V

All the bits in this register are Intel TXT lockable.

Bit	Type	Default Value	RST Type	Description
15:8	RO_V	0x5	default/uncore	**GMS:** This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled. BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0. 00h:0MB 01h:32MB 02h:64MB 03h:96MB 04h:128MB 05h:160MB (default) 06h:192MB 07h:224MB 08h:256MB 09h:288MB 0Ah:320MB 0Bh:352MB 0Ch:384MB 0Dh:416MB 0Eh:448MB 0Fh:480MB 10h:512MB 11h - 1Fh: Reserved 20h:1024MB 21h - 2Fh: Reserved 30h:1536MB 31h - 3Eh: Reserved 3Fh: 2016MB 40h - FFh: Reserved Hardware functionality in case of programming this value to Reserved is not guaranteed.

Bit	Type	Default Value	RST Type	Description
7:6	RO_V	0x0	default/uncore	**GGMS:** This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware will derive the base of GSM from DSM only using the GSM size programmed in the register. Hardware functionality in case of programming this value to Reserved is not guaranteed. 0x0:No Preallocated Memory 0x1:2MB of Preallocated Memory 0x2:4MB of Preallocated Memory 0x3:8MB of Preallocated Memory
2:2	RO_V	0x0	default/uncore	**VAMEN:** Enables the use of the iGFX engines for Versatile Acceleration. 1 - iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 048000h. 0 - iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h.
1:1	RO_V	0x0	default/uncore	**IVD:** 0: Enable. Device 2 IGD claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1: Disable. Device 2 IGD does not claim VGA cycles Mem and IO, and the Sub- Class Code field within Device 2 function 0 Class Code register is 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field bits 7:3 of this register pre-allocates no memory. This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override CAPID0AIGD 1 or via a register DEVEN3 0. 0:Enable 1:Disable
0:0	RO_V	0x0	default/uncore	**GGCLCK:** When set to 1b, this bit will lock all bits in this register.

MPGFXTRK_CR_MTOUUD_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x108080

Size: 64 bits

Access: RO_V

This 64 bit register defines the Top of Upper Usable DRAM.

Configuration software must set this value to TOM minus all ME stolen memory if reclaim is disabled. If reclaim is enabled, this value must be set to reclaim limit 1byte, 1MB aligned, since reclaim limit is 1MB aligned. Address bits 19:0 are assumed to be 0000000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than or equal to 4GB.

BIOS Restriction: Minimum value for TOUUD is 4GB.

These bits are Intel TXT lockable.

Bit	Type	Default Value	RST Type	Description
38:20	RO_V	0x0	default/uncore	**TOUUD:** This register contains bits 38 to 20 of an address one byte above the maximum DRAM memory above 4G that is usable by the operating system. Configuration software must set this value to TOM minus all ME stolen memory if reclaim is disabled. If reclaim is enabled, this value must be set to reclaim limit 1MB aligned since reclaim limit 1byte is 1MB aligned. Address bits 19:0 are assumed to be 0000000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than 4GB.
0:0	RO_V	0x0	default/uncore	**LOCK:** This bit will lock all writeable settings in this register, including itself.

MPGFXTRK_CR_MBDSM_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x1080c0

Size: 32 bits

Access: RO_V

This register contains the base address of graphics data stolen DRAM memory. BIOS determines the base of graphics data stolen memory by subtracting the graphics data stolen memory size PCI Device 0 offset 52 bits 7:4 from TOLUD PCI Device 0 offset BC bits 31:20.

Bit	Type	Default Value	RST Type	Description
31:20	RO_V	0x0	default/uncore	**BDSM:** This register contains bits 31 to 20 of the base address of stolen DRAM memory. BIOS determines the base of graphics stolen memory by subtracting the graphics stolen memory size PCI Device 0 offset 52 bits 6:4 from TOLUD PCI Device 0 offset BC bits 31:20.
0:0	RO_V	0x0	default/uncore	**LOCK:** This bit will lock all writeable settings in this register, including itself.

MPGFXTRK_CR_MBGSM_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x108100

Size: 32 bits

Access: RO_V

This register contains the base address of stolen DRAM memory for the GTT. BIOS determines the base of GTT stolen memory by subtracting the GTT graphics stolen memory size PCI Device 0 offset 52 bits 9:8 from the Graphics Base of Data Stolen Memory PCI Device 0 offset B0 bits 31:20.

Bit	Type	Default Value	RST Type	Description
31:20	RO_V	0x1	default/uncore	**BGSM:** This register contains the base address of stolen DRAM memory for the GTT. BIOS determines the base of GTT stolen memory by subtracting the GTT graphics stolen memory size PCI Device 0 offset 50 bits 7:6 from the Graphics Base of Data Stolen Memory PCI Device 0 offset B0 bits 31:20.
0:0	RO_V	0x0	default/uncore	**LOCK:** This bit will lock all writeable settings in this register, including itself.

MPGFXTRK_CR_MGCMD_REG_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x108300

Size: 32 bits

Access: RO_V/RO/WO

Register to control remapping hardware. If multiple control fields in this register need to be modified, software must serialize the modifications through multiple writes to this register.

Bit	Type	Default Value	RST Type	Description
31:31	RO_V	0x0	default/uncore	**TE:** Software writes to this field to request hardware to enabledisable DMA-remapping: 0: Disable DMA remapping 1: Enable DMA remapping Hardware reports the status of the translation enable operation through the TES field in the Global Status register. There may be active DMA requests in the platform when software updates this field. Hardware must enable or disable remapping logic only at determinstic transaction boundaries, so that any in-flight transaction is either subject to remapping or not at all. Hardware implementations supporting DMA draining must drain any in-flight DMA readwrite requests queued within the Root-Complex before completing the translation enable command and reflecting the status of the command through the TES field in the Global Status register. The value returned on a read of this field is undefined.
30:30	WO	0x0	default/uncore	**SRTP:** Software sets this field to setupdate the root-entry table pointer used by hardware. The root-entry table pointer is specified through the Root-entry Table Address RTAREG register. Hardware reports the status of the "Set Root Table Pointer" operation through the RTPS field in the Global Status register. The "Set Root Table Pointer" operation must be performed before enabling or re-enabling after disabling DMA remapping through the TE field. After a "Set Root Table Pointer" operation, software must globally invalidate the context cache and then globally invalidate of IOTLB. This is required to ensure hardware uses only the remapping structures referenced by the new root table pointer, and not stale cached entries.

Bit	Type	Default Value	RST Type	Description
				While DMA remapping hardware is active, software may update the root table pointer through this field. However, to ensure valid in-flight DMA requests are deterministically remapped, software must ensure that the structures referenced by the new root table pointer are programmed to provide the same remapping results as the structures referenced by the previous root-table pointer. Clearing this bit has no effect. The value returned on read of this field is undefined.
29:29	RO	0x0	default/uncore	**SFL:** This field is valid only for implementations supporting advanced fault logging. Software sets this field to request hardware to setupdate the fault-log pointer used by hardware. The fault-log pointer is specified through Advanced Fault Log register. Hardware reports the status of the 'Set Fault Log' operation through the FLS field in the Global Status register. The fault log pointer must be set before enabling advanced fault logging through EAFL field. Once advanced fault logging is enabled, the fault log pointer may be updated through this field while DMA remapping is active. Clearing this bit has no effect. The value returned on read of this field is undefined.
28:28	RO	0x0	default/uncore	**EAFL:** This field is valid only for implementations supporting advanced fault logging. Software writes to this field to request hardware to enable or disable advanced fault logging: 0: Disable advanced fault logging. In this case, translation faults are reported through the Fault Recording registers. 1: Enable use of memory-resident fault log. When enabled, translation faults are recorded in the memory-resident log. The fault log pointer must be set in hardware through the SFL field before enabling advanced fault logging. Hardware reports the status of the advanced fault logging enable operation through the AFLS field in the Global Status register. The value returned on read of this field is undefined.

Bit	Type	Default Value	RST Type	Description
27:27	RO	0x0	default/uncore	**WBF:** This bit is valid only for implementations requiring write buffer flushing. Software sets this field to request that hardware flush the Root-Complex internal write buffers. This is done to ensure any updates to the memory-resident remapping structures are not held in any internal write posting buffers. Hardware reports the status of the write buffer flushing operation through the WBFS field in the Global Status register. Clearing this bit has no effect. The value returned on a read of this field is undefined.
26:26	RO_V	0x0	default/uncore	**QIE:** This field is valid only for implementations supporting queued invalidations. Software writes to this field to enable or disable queued invalidations. 0: Disable queued invalidations. 1: Enable use of queued invalidations. Hardware reports the status of queued invalidation enable operation through QIES field in the Global Status register. The value returned on a read of this field is undefined.
25:25	RO_V	0x0	default/uncore	**IRE:** This field is valid only for implementations supporting interrupt remapping. 0: Disable interrupt-remapping hardware 1: Enable interrupt-remapping hardware Hardware reports the status of the interrupt remapping enable operation through the IRES field in the Global Status register. There may be active interrupt requests in the platform when software updates this field. Hardware must enable or disable interrupt-remapping logic only at deterministic transaction boundaries, so that any in-flight interrupts are either subject to remapping or not at all. Hardware implementations must drain any in-flight interrupts requests queued in the Root-Complex before completing the interrupt-remapping enable command and reflecting the status of the command through the IRES field in the Global Status register. The value returned on a read of this field is undefined.

Bit	Type	Default Value	RST Type	Description
24:24	WO	0x0	default/uncore	**SIRTP:** This field is valid only for implementations supporting interrupt-remapping. Software sets this field to setupdate the interrupt remapping table pointer used by hardware. The interrupt remapping table pointer is specified through the Interrupt Remapping Table Address IRTAREG register. Hardware reports the status of the 'Set Interrupt Remap Table Pointer' operation through the IRTPS field in the Global Status register. The 'Set Interrupt Remap Table Pointer' operation must be performed before enabling or re-enabling after disabling interrupt-remapping hardware through the IRE field. After a 'Set Interrupt Remap Table Pointer' operation, software must globally invalidate the interrupt entry cache. This is required to ensure hardware uses only the interrupt-remapping entries referenced by the new interrupt remap table pointer, and not any stale cached entries. While interrupt remapping is active, software may update the interrupt remapping table pointer through this field. However, to ensure valid in-flight interrupt requests are deterministically remapped, software must ensure that the structures referenced by the new interrupt remap table pointer are programmed to provide the same remapping results as the structures referenced by the previous interrupt remap table pointer. Clearing this bit has no effect. The value returned on a read of this field is undefined.
23:23	RO_V	0x0	default/uncore	**CFI:** This field is valid only for Intel64 implementations supporting interrupt-remapping. Software writes to this field to enable or disable Compatibility Format interrupts on Intel64 platforms. The value in this field is effective only when interrupt-remapping is enabled and Extended Interrupt Mode x2APIC mode is not enabled. 0: Block Compatibility format interrupts. 1: Process Compatibility format interrupts as pass-through bypass interrupt remapping. Hardware reports the status of updating this field through the CFIS field in the Global Status register. The value returned on a read of this field is undefined.

MPGFXTRK_CR_MEMRR_BASE_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x108340

Size: 64 bits

Access: RO_V

The EMRR range is used to protect Xucode memory from unauthorized reads and writes. Any IO access to this range is aborted. This register controls the location of the EMRR range by indicating its starting address.

It functions in tandem with the EMRR mask register.

Bit	Type	Default Value	RST Type	Description
38:12	RO_V	0x0	default/uncore	**RANGE_BASE:** This field corresponds to bits 38:12 of the base address memory range which is allocated to EMRR memory.

MPGFXTRK_CR_MEMRR_MASK_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x108380

Size: 64 bits

Access: RO_V

This register controls the size of the EMRR range by indicating which address bits must match the EMRR base register value.

Bit	Type	Default Value	RST Type	Description
38:12	RO_V	0x0	default/uncore	**RANGE_MASK:** This field indicates which address bits must match EMRR base in order to qualify as an EMRR access.
11:11	RO_V	0x0	default/uncore	**RANGE_EN:** Indicates whether the EMRR range is enabled and valid.
10:10	RO_V	0x0	default/uncore	**LOCK:** Setting this bit locks all writeable settings in this register, including itself.

MPMCARB_CR_EDRAMCAP_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x120010

Size: 32 bits

Access: RO_FW

Describes the presence and capabilities of the EDRAM cache.

This register's contents can be changed by iGfx. Uncore hardware should not use any EDRAM related information from this register.

Bit	Type	Default Value	RST Type	Description
31:1	RO_FW	0x0	default/uncore	**EDRAM Capability:** These bits are reserved to indicate capabilities of EDRAM cache size, assoc, SPL size, etc
0:0	RO_FW	0x0	default/uncore	**EDRAM Enabled:** This bit is set if there is an EDRAM cache present in the package

PCU Registers

PCU_CR_GT_THREAD_STATUS_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x13805c

Size: 32 bits

Access: RO_V

Per-thread status register. Note that hardware prevents this register from being written if the corresponding thread is disabled. Ucode cannot change any fields in this register from another thread when this thread is disabled.

Bit	Type	Default Value	RST Type	Description
31:31	RO_V	0x0	default/uncore	**Thread Active(THREAD_ACTIVE):** Virtual signal from the ROB signaling that the thread is active.
30:30	RO_V	0x0	default/uncore	**Vote Request(VOTE_REQUEST):** The PCU HW will compute this field which indicates that the thread requests a P-State voting right. This bit will be set on TC0-TC1 and cleared on TC1E-TC7. Also, there is a promote all TC1 to TC1E flag which is taken into account.
18:16	RO_V	0x7	default/uncore	**Thread Wish C-State Result(THREAD_WISH_RESULT):** This field contains the PCU's response to the Thread's C-State Wish. It is combinatorical logic, calculated at PCU HW, equals to the minimum between ThreadWishState and this core's IOSliceDemotedCState. It can only be CC0, CC3, CC6.

Bit	Type	Default Value	RST Type	Description
15:12	RO_V	0xf	default/uncore	**Thread Wish Sub-State(THREAD_WISH_SUB_STATE):** This field specifies the Thread C-State Sub-State that the thread wants to be in. It is updated by the thread during the WISH phase. Microcode does not interpret these values; the interpretation is done in the PCU. Microcode DOES NOT clip it, so actually any value is possible. Clipping is done at PCODE. Sub-States for TC1 0000b TC1KEEPVR 0001b TC1LOOSEVR C1E Sub-States for TC6 0000b TC6SHORTIRTLMSR 0001b TC6LONGIRTLMSR Sub-States for TC7 0000b TC7SHORTIRTLMSRTC7GRADUALLLCSHUTDOWN 0001b TC7LONGIRTLMSRTC7GRADUALLLCSHUTDOWN 0010b TC7SHORTIRTLMSRTC7CLOSELLCATONCE C7S 0011b TC7LONGIRTLMSRTC7CLOSELLCATONCE C7S Sub-States for RC6RC7 0000b RC6
11:8	RO_V	0xf	default/uncore	**Thread Wish C-State(THREAD_WISH_STATE):** This field specifies the Thread C-State that the thread wants to be in. It is updated by the thread during the WISH phase. UCODE will update this field with the parameters of the MWAIT instruction.

Bit	Type	Default Value	RST Type	Description
6:4	RO_V	0x0	default/uncore	**Thread Power Down State(THREAD_TPD_STATE):** MicrocodeGT writeable field, specifying the CPD core power down state. The default value for the Thread Power Down TPD State is Normal 000b. The possible values are: Value TPD State 3'b000 Normal 3'b001 TPD, due to GV 3'b010 TPD, due to TT1 3'b011 TPD, due to S-State other reserved
2:0	RO_V	0x7	default/uncore	**Thread C- State(THREAD_STATE):** MicrocodeGT writeable field, specifying the CC-State where microcode is. The default value of the Thread C-State is CRST 111b. The possible values are: Value C-State 3'b000 CC0RC0 includes CC1RC1 and CPD states 3'b001 not in use, as CC1RC1 are not signaled 3'b010 CC3RC3 3'b011 CC6RC6 3'b100 CC7RC7 -- This is not in use for Gesher. 3'b111 CRST. The reset value of this register. other reserved NOTE: For unsupported C-states, PCODE will demote the request to the next higher power C-state.

PCU_CR_GT_CORE_STATUS_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x138060

Size: 32 bits

Access: RO_V

Per-core status register.

Bit	Type	Default Value	RST Type	Description
31:31	RO_V	0x0	default/uncore	**Core Active(CORE_ACTIVE):** Virtual signal from the ROB, signaling that the core is active. During CORERESET, ROB will indicate that the core is active but this indication will be filtered by the HW i.e. COREACTIVE will remain 0b.
30:30	RO_V	0x0	default/uncore	**Wakeup Request(WAKEUP_REQUEST):** Virtual signal from the NCUGTFIFO specifying that there is an event pending for the IAGT Core. This can only happen if the core blocked events. PCODE can set this bit by writing to the PCODEWAKEUPREQUEST IO Register. In use by the following: Set by virtual signal from the NCU, when the core is asleep, and need to wake it up. Cleared by PCU HW as part of the wakeup flow. Can be set by PCODE in order to signal TTT expire Always Running APIC Timer. When rise, no matter why, issues C-State Fast Path event for this core.
28:28	RO_V	0x1	default/uncore	**Core in C3/C6(CORE_IN_C3_C6):** This bit indicates that the dispatcher has put a core in C3C6. NOTE: On wakeup, this bit must de-asserted after at least COREACTIVE is asserted or CORESTATE was cleared.
27:27	RO_V	0x0	default/uncore	**Probe Mode Done Indication(PROBE_MODE_DONE):** This bit is used by UCODE to inform the PCU that the Probe Mode sequence that it was running is done.

Bit	Type	Default Value	RST Type	Description
26:26	RO_V	0x0	default/uncore	**Disable Wakeup Request(DISABLE_WAKEUP_REQ):** This bit is only applicable to the GT core. When set, any GT wake request is masked and will not trigger a wakeup.
25:25	RO_V	0x0	default/uncore	**S1 acknowledge from PMA(S1_ACK):** This bit is set by an UpS virtual signal from the PMA when the core has acknowledged the S1 CPD request from pcode.
24:24	RO_V	0x1	default/uncore	**Block Request(PM_BLOCK_REQ):** This field is not used by GT cores.
23:23	RO_V	0x0	default/uncore	**RFO Status(RFO_EN):** This field only has meaning for the GT register instance. It is a don't care for the IA register instances. For GT: This bit indicates the status of RFOs from the core. If it is set, RFOs are enabled, and if it is clear, RFOs are disabled.
15:12	RO_V	0xf	default/uncore	**Core Wish Sub C-State(CORE_WISH_SUB_STATE):** This field specifies the coordinated Sub C-State that the core wants to be in. In case the two threads have different wish states, the field should contain sub C-state of the thread with the smaller wish state. In case the two threads have identical wish states, this field should contain a bit-wise AND of each thread's wish sub C-state. The thread wish sub C-state is given in PCUCRTHREADSTATUS.
11:8	RO_V	0xf	default/uncore	**Core Wish C-State(CORE_WISH_STATE):** This field specifies the coordinated Core C-State that the core wants to be in. It is defined as the minimum of the thread wish CST in case two threads are active. The thread wish state is given in PCUCRTHREADSTATUS.

Bit	Type	Default Value	RST Type	Description
6:4	RO_V	0x0	default/uncore	**Core Power Down State(CORE_CPD_STATE):** MicrocodeGT writeable field, specifying the CPD core power down state. The default value for the Core Power Down CPD State is Normal 000b. The possible values are: Value CPD State 3'b000 Normal 3'b001 CPD, due to GV 3'b010 CPD, due to TT1 3'b011 CPD, due to S-State 3'b100 CPD, S1-S 3'b101 CPD, due to IA GV other reserved
2:0	RO_V	0x7	default/uncore	**Core C-State(CORE_STATE):** MicrocodeGT writeable field, specifying the CC-State where microcode is. The default value of the Core C-State is CRST 111b. HW will clear this field to 000b on C-State exit when Core clock is ungated. The possible values are: Value C-State 3'b000 CC0RC0 includes CC1RC1 and CPD states 3'b001 not in use, as CC1RC1 are not signaled 3'b010 CC3RC3 3'b011 CC6RC6 3'b100 CC7RC7 -- This is not in use for Gesher. 3'b111 CRST. The reset value of this register. other reserved NOTE: For unsupported C-states, PCODE will demote the request to the next higher power C-state.

PCU_CR_GT_SLICE_INFO_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x138064

Size: 32 bits

Access: RO_V/RW/RW_V

Control and Status register for GT partial slice modes.

Bit	Type	Default Value	RST Type	Description
7:5	RW	0x7	default/uncore	**Slice Selection(LSLICESEL):** Indicates which GTT slices to power at the next C6 exit. 00x: Power only GT slice 0 01x: Power GT slices 0 and 1 1xx: Power GT slices 0, 1, and 2 The driver must not write to this register directly, unless it can guarantee the render pipe is flushed. Generally the driver will write to GPMunit MMIO register instead.
4:4	RW	0x0	default/uncore	**Auto wake(C6_ENTRANCE):** Indicates whether pcode should do the slice status change via a CPD or on the next C6 event. 0: Do immediately, with pcode generating a new ratio change 1: Wait until the next C6 The Autowake bit of this register is only sampled when this bit is set to 1.
3:3	RW_V	0x0	default/uncore	**Auto wake(AUTOWAKE):** Control automatic wake of GT 0: Normal mode; wake when GT indicates FIFO not empty 1: Wake GT immediately after C6 entry PCU will self-clear this bit after the next wake from C6

Bit	Type	Default Value	RST Type	Description
2:0	RO_V	0x0	default/uncore	**Slice Status(LSLICESTAT):** Status of GT power planes 000: GT is powered off C6 or not yet booted 001: GT has slice 0 powered 011: GT has slices 0 and 1 powered 111: GT has slices 0, 1, and 2 powered

PCU_CR_GT_READ_LLC_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x138068

Size: 32 bits

Access: RO_V

This register is the sum of the cycles GT has read LLC. It contains a 32-bit accumulation of data sent via the Pushbus. Values exceeding 32 bits will wrap around.

Bit	Type	Default Value	RST Type	Description
31:0	RO_V	0x0	default/uncore	**Data(DATA):** Number of Cycles

PCU_CR_GT_WRITE_LLC_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x13806c

Size: 32 bits

Access: RO_V

This register is the sum of the cycles GT has written LLC. It contains a 32-bit accumulation of data sent via the Pushbus. Values exceeding 32 bits will wrap around.

Bit	Type	Default Value	RST Type	Description
31:0	RO_V	0x0	default/uncore	**Data(DATA):** Number of Cycles

PCU_CR_GT_READ_EDRAM_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x138070

Size: 32 bits

Access: RO_V

This register is the sum of the cycles GT has read EDRAM. It contains a 32-bit accumulation of data sent via the Pushbus. Values exceeding 32 bits will wrap around.

Bit	Type	Default Value	RST Type	Description
31:0	RO_V	0x0	default/uncore	**Data(DATA):** Number of Cycles

PCU_CR_GT_WRITE_EDRAM_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x138074

Size: 32 bits

Access: RO_V

This register is the sum of the cycles GT has written EDRAM. It contains a 32-bit accumulation of data sent via the Pushbus. Values exceeding 32 bits will wrap around.

Bit	Type	Default Value	RST Type	Description
31:0	RO_V	0x0	default/uncore	**Data(DATA):** Number of Cycles

PCU_CR_GT_RW_DRAM_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x138078

Size: 32 bits

Access: RO_V

This register is the sum of the cycles GT has read or written DRAM. It contains a 32-bit accumulation of data sent via the Pushbus. Values exceeding 32 bits will wrap around.

Bit	Type	Default Value	RST Type	Description
31:0	RO_V	0x0	default/uncore	**Data(DATA):** Number of Cycles

PCU_CR_GT_THREAD_P_REQ_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x13807c

Size: 32 bits

Access: RW

Thread Target P-state Value. All values in this register are updated by Ucode as a result of WRMSR requests.

Bit	Type	Default Value	RST Type	Description
31:31	RW	0x0	default/uncore	**Turbo Disable(TURBO_DISABLE):** The Turbo Disable bit is determined by SW. SW access to IA32PERFCTLMSRTURBODIS is routed to this field by Ucode. NOTE: If Turbo is disabled for ANY thread, it will prevent turbo for ALL threads.
30:24	RW	0x0	default/uncore	**Maximum P-state Request(P_STATE_REQ):** This field indicates the maximum P-State request in units of 100MHz. It is determined by SW. SW access to IA32PERFCTLMSRPREQ is routed to this field by Ucode.

Bit	Type	Default Value	RST Type	Description
23:18	RW	0x0	default/uncore	**P-State Offset(P_STATE_OFFSET):** This field defines the number of steps that Energy Efficient P-State is allowed to fall in units of 100 MHz. It is determined by Ucode as follows: PSTATEOFST PSTCONFIGCONTROLMSRPSTATEOFST
17:14	RW	0x0	default/uncore	**Energy Efficiency Policy(ENERGY_EFFICIENCY_POLICY):** The energy efficiency policy is determined by SW. SW access to IA32ENERGYPERFORMANCEBIASMSRPERFPOLICY is routed to this field by Ucode.

PCU_CR_GT_ARAT_TTT_LOW_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x138080

Size: 32 bits

Access: RW

Always Running APIC Timer, TTT Timer Target Time value, for the GT core. This value is an absolute desired wakeup time. PCU will wake up the GT core when the TSC will reach the TTT value. The APIC timer is divided into two registers.

Bit	Type	Default Value	RST Type	Description
31:0	RW	0xffffffff	default/uncore	**DATA:** The low 32 bits of the TTT. GT will update this field with its current TTT value before entering C-State.

PCU_CR_GT_ARAT_TTT_HIGH_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x138084

Size: 32 bits

Access: RW

Always Running APIC Timer, TTT Timer Target Time value, for the GT core. This value is an absolute desired wakeup time. PCU will wake up the GT core when the TSC will reach the TTT value. The APIC timer is divided into two registers.

Bit	Type	Default Value	RST Type	Description
28:0	RW	0x1fffffff	default/uncore	**DATA:** The upper 29 bits of the TTT. GT will update this field with its current TTT value before entering C-State.

PCU_CR_GTC6_PREWAKE_TIMER_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x138088

Size: 32 bits

Access: RW

This register contains the enable and value for the prewake timer that the GT driver can program to prewake GT from C6.

Bit	Type	Default Value	RST Type	Description
15:15	RW	0x0	default/uncore	**TMR_ENABLE:** Enable the GT prewake timer. The driver sets this bit to 1 to enable the timer.
14:0	RW	0x0	default/uncore	**TMR_VALUE:** Prewake timer value in microseconds.

PCU_CR_GT_GFX_RC6_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x138108

Size: 32 bits

Access: RO_FW

This register contains the total RC6 residency time that GT was in since boot. The counter will wrap around. The time is given in units of 1.28 uSec.

Bit	Type	Default Value	RST Type	Description
31:0	RO_FW	0x0	default/uncore	**Residency Time(RC6):** Value

PCU_CR_GTDRIVER_MAILBOX_INTERFACE_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x138124

Size: 32 bits

Access: RW1S/RW_V

Control and Status register for the GFX-DRIVER-to-PCODE mailbox. This mailbox is implemented as a means for tuning parameters for specific GFX workloads.

This register is used in conjunction with GTDRIVERMAILBOXDATA.

Bit	Type	Default Value	RST Type	Description
31:31	RW1S	0x0	default/uncore	**Run/Busy Indicator(RUN_BUSY):** SW may write to the mailbox registers only when RUNBUSY is cleared 0b. Setting RUNBUSY to 1b will create a Fast Path event. After setting this bit, SW will poll this bit until it is cleared. Alternatively, PCODE can generate an interrupt to SW via GTDRIVERP2GEVENTS. PCODE will clear RUNBUSY after updating the mailbox registers with the result and error code.
28:8	RW_V	0x0	default/uncore	**Address Control(ADDR_CNTL):** This field contains the address associated with specific commands.

Bit	Type	Default Value	RST Type	Description
7:0	RW_V	0x0	default/uncore	**Command Code(COMMAND):** This field contains the SW request command or the PCODE response code, depending on the setting of RUNBUSY. Command Encodings: 00h ZERO 01h CMD_CONFIG 02h WRITE_PCS 03h READ_PCS 04h Unavailable 05h Unavailable 06h Unavailable 07h Unavailable 08h WRITE_MIN_FREQUENCY_TABLE 09h READ_MIN_FREQUENCY_TABLE 0Ah CLEAR_RCX_RESIDENCE_COUNTERS 0Bh READ_RING_RATIOS 0Ch READ_OVERCLOCK_PARAMS 0Dh READ_PCU_MISC_CONFIG 0Eh WRITE_PCU_MISC_CONFIG 0Fh READ_PKGC_PMREQ_FORMAT 10h Unavailable 11h Unavailable 12h Unavailable 13h WRITE_LLC_MIN_OPENWAYS 14h READ_LLC_MIN_OPENWAYS 15h RD_GT_SLICE_RECOMMENDATION 16h READ_REQUESTED_DUTY_CYCLE 17h DE_WRITE_FREQ_REQ 18h DISPLAY_FREQ_CHANGE_REQ 19h DISPLAY_IPS_CONTROL 1Ah DYNAMIC_DUTY_CYCLE_CONTROL 1Bh Unavailable 1Ch Unavailable 1Dh Unavailable

PCU_CR_GTDRIVER_MAILBOX_DATA0_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x138128

Size: 32 bits

Access: RW_V

Data register for the GFX-DRIVER-to-PCODE mailbox. This mailbox is implemented as a means for tuning parameters for specific GFX workloads.

This register is used in conjunction with GTDRIVERMAILBOXINTERFACE.

Bit	Type	Default Value	RST Type	Description
31:0	RW_V	0x0	default/uncore	**Data(DATA):** This field contains the data associated with specific commands.

PCU_CR_GTDRIVER_MAILBOX_DATA1_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x13812c

Size: 32 bits

Access: RW_V

Data register for the GFX-DRIVER-to-PCODE mailbox. This mailbox is implemented as a means for tuning parameters for specific GFX workloads.

This register is used in conjunction with GTDRIVERMAILBOXINTERFACE.

Bit	Type	Default Value	RST Type	Description
31:0	RW_V	0x0	default/uncore	**Data(DATA):** This field contains the data associated with specific commands.

PCU_CR_GT_PM_CONFIG_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x138140

Size: 32 bits

Access: RW

Bit	Type	Default Value	RST Type	Description
0:0	RW	0x0	default/uncore	**Reserved**

PCU_CR_D_COMP_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x138144

Size: 32 bits

Access: RW1S/RO_V/RW

Display COMP control

Bit	Type	Default Value	RST Type	Description
9:9	RO_V	0x0	default/uncore	**Display IO Comp in progress(COMP_IN_PROGRESS):** Status bit to tell when DComp is in progress. '1 DComp in progress, '0 DComp is idle
8:8	RW1S	0x0	default/uncore	**Force a COMP cycle(COMP_FORCE):** Writing '1' to this field triggers a COMP cycle. HW will reset this bit when the COMP cycle starts.
4:1	RW	0x8	default/uncore	**Periodic COMP Interval(COMP_INTERVAL):** This field indicates the period of RCOMP. The default value of Dh corresponds to 88 ms.
0:0	RW	0x0	default/uncore	**COMP Disable(COMP_DISABLE):** Disable periodic COMP cycles 0b Enabled 1b Disabled

PCU_CR_P_STATE_LIMITS_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x138148

Size: 32 bits

Access: RW_KL/RW_L

This register allows SW to limit the maximum frequency allowed during run-time.

PCODE will sample this register in slow loop.

Bit	Type	Default Value	RST Type	Description
31:31	RW_KL	0x0	default/uncore	**Lock(LOCK):** This bit will lock all settings in this register.
15:8	RW_L	0x0	default/uncore	**P-State Min(PSTT_MIN):** PG1 ratio used to be an offset from P1, now absolute to avoid avoid interaction with ConfigTDP. This is clipped to be greater than or equal to Pn or Pm when LPM is enabled, and less than or equal to P1 after any adjustments by flex ratio, ConfigTDP, etc.
7:0	RW_L	0xff	default/uncore	**P-State Limitation(PSTT_LIM):** This field indicates the maximum IA frequency limit allowed during run-time.

PCU_CR_GT_RATIOS_OVERRIDE_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x13814c

Size: 32 bits

Access: RW

Non-zero values here will allow GT driver to directly request IA and CLR ratios, without regards to the normal gfxmailbox min frequency tables. Ratios written here will be subject to the same limit clipping algorithms that are used for other ratio checks. Zero values here default means this override mechanism is disabled, and the normal gfxmailbox min frequency tables will be used. This register is written by GT driver and read by pcode in the slowloop.

Bit	Type	Default Value	RST Type	Description
15:8	RW	0x0	default/uncore	**CLR_MIN_RATIO_REQUEST:** GT driver's minimum requested ratio for CLR a.k.a. Ring domain. A value of zero here means no override request i.e. normal gfxmailbox min frequency table will be used.
7:0	RW	0x0	default/uncore	**IA_MIN_RATIO_REQUEST:** GT driver's minimum requested ratio for IA domain. A value of zero here means no override request i.e. normal gfxmailbox min frequency table will be used.

PCU_CR_GRAPHICS_INTERRUPT_RESPONSE_TIME_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x138150

Size: 32 bits

Access: RW

The coordinated Package-Additive above the core Graphics Interrupt Response Time is used for BIOS runtime control. This setting affects the selected package state. It is reflected to the PCH as part of the PMREQ message for chipset usage as well.

This register may be changed dynamically due to platform events ACDC, etc.

PCODE will sample this at slow loop.

Bit	Type	Default Value	RST Type	Description
15:15	RW	0x0	default/uncore	**Valid(VALID):** This field qualifies the validity of the Value field in this register.
12:10	RW	0x0	default/uncore	**Multiplier(MULTIPLIER):** This field indicates the unit of measurement that is defined for the Value field in this register.
9:0	RW	0x0	default/uncore	**Value(VALUE):** The Interrupt Response Time Limit is given in units defined in the Multipler field of this register.

PCU_CR_EDRAM_PM_CONTROL_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x138154

Size: 32 bits

Access: RW

Interface for SW control of eDRAM.

Bit	Type	Default Value	RST Type	Description
31:31	RW	0x0	default/uncore	**MODE:** 0 PCU takes full control control default 1 SW explicitly takes control while PCU makes best efforts to obey the SWs hint. There is no specific guarantee of a response time on SWs hint. Note that SW can toggle this mode bit at any time.
30:30	RW	0x0	default/uncore	**POLICY:** 0 SW requests PCU to control eDRAM to operate in WB mode default 1 SW requests PCU to trigger eDRAM to operate in WT mode completely. All dirty superlines are cleaned and not allowed for modification. Latency of completion can vary. This SW hint is effective regardless of MODE setting i.e. bit 31 of this register.
29:28	RW	0x0	default/uncore	**PKGC_FLUSH_LEVEL:** 00 OK to flush only from PkgC3 or deeper. default 01 OK to flush only from PkgC6 or deeper. 10 OK to flush only from PkgC7 or deeper. 11 Do not flush. This SW hint is effective regardless of MODE setting i.e. bit 31 of this register.

Bit	Type	Default Value	RST Type	Description
15:0	RW	0x0	default/uncore	**WAYS_EN:** This is a bitvector containing 1 bit for each of the 16 ways. 0 flush the way for powerdown 1 power up the way. eDRAM off is possible only if these bits are all zero. Clearing individual bits does not require any special action for PCU if any of 16 bits is set i.e. pcode actually uses an OR across all of these bits to determine whether to turn eDRAM ON. These control bits are effective only if MODE bit is set i.e. bit 31 of this register 1.

PCU_CR_PRIP_TURBO_PLCY_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x138158

Size: 32 bits

Access: RW

The PRIMARYPLANETURBOPOWERPOLICY and SECONDARYPLANETURBOPOWERPOLICY are used together to balance the power budget between the two power planes.

The power plane with the higher policy will get a higher priority. The default values for these registers give a higher priority to the secondary power plane.

Bit	Type	Default Value	RST Type	Description
4:0	RW	0x0	default/uncore	**Primary Plane Turbo Policy(PRIPTP):** Priority Level. A higher number implies a higher priority.

PCU_CR_SECP_TURBO_PLCY_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x13815c

Size: 32 bits

Access: RW

The PRIMARYPLANETURBOPOWERPOLICY and SECONDARYPLANETURBOPOWERPOLICY are used together to balance the power budget between the two power planes.

The power plane with the higher policy will get a higher priority. The default values for these registers give a higher priority to the secondary power plane.

Bit	Type	Default Value	RST Type	Description
4:0	RW	0x10	default/uncore	**Secondary Plane Turbo Policy(SECPTP):** Priority Level. A higher number implies a higher priority.

PCU_CR_GTDRIVER_P2G_EVENTS_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x138160

Size: 32 bits

Access: RW1C

This extended capability allows PCODE to send an interrupt notification upon completion of a mailbox command. It is enabled via the GFX Driver Mailbox.

PCODE will set the appropriate bit in this register to 1b, and will then write to 0.2.0.GTTMMADR.PIMPCUMBOXE.

The GFX Driver will clear the appropriate bit in this register by writing a 1 to the bit.

Bit	Type	Default Value	RST Type	Description
7:7	RW1C	0x0	default/uncore	**Event 7(EVENT7):** Placeholder for Event
6:6	RW1C	0x0	default/uncore	**Event 6(EVENT6):** Placeholder for Event
5:5	RW1C	0x0	default/uncore	**Event 5(EVENT5):** Placeholder for Event
4:4	RW1C	0x0	default/uncore	**Event 4(EVENT4):** Placeholder for Event
3:3	RW1C	0x0	default/uncore	**Event 3(EVENT3):** Placeholder for Event
2:2	RW1C	0x0	default/uncore	**Event 2(EVENT2):** Placeholder for Event
1:1	RW1C	0x0	default/uncore	**Event 1(EVENT1):** Placeholder for Event
0:0	RW1C	0x0	default/uncore	**Event 0(EVENT0):** This event indicates that the command previously sent by the GFX Driver via the Mailbox mechanism is complete.

PCU_CR_GTDRIVER_G2P_EVENTS_0_2_0_GTTMMADR

B/D/F/Type: 0/2/0/GTTMMADR

Address Offset: 0x138164

Size: 32 bits

Access: RW1S

This extended capability allows the GFX Driver to send a request to PCODE.

The GFX Driver will set the appropriate bit in this register to 1b when it wants to generate an event to PCODE. This will generate a Fast Path event.

PCODE will clear the appropriate bit in this register after servicing the request.

Bit	Type	Default Value	RST Type	Description
7:7	RW1S	0x0	default/uncore	**Event 7(EVENT7):** Placeholder for Event
6:6	RW1S	0x0	default/uncore	**Event 6(EVENT6):** Placeholder for Event
5:5	RW1S	0x0	default/uncore	**Event 5(EVENT5):**
4:4	RW1S	0x0	default/uncore	**Event 4(EVENT4):** Placeholder for Event
3:3	RW1S	0x0	default/uncore	**Event 3(EVENT3):** Placeholder for Event
2:2	RW1S	0x0	default/uncore	**Event 2(EVENT2):** Placeholder for Event
1:1	RW1S	0x0	default/uncore	**Event 1(EVENT1):** Placeholder for Event
0:0	RW1S	0x0	default/uncore	**Event 0(EVENT0):** Placeholder for Event

GSA Registers

Address Space	Address	Symbol	Name
MMIO: 0/2/0	130040h	LCPLL_CTL	LCPLL Control
MMIO: 0/2/0	130044h	GTSP1_0_2_0_GTTMMADR	GT Scratch Pad 1
MMIO: 0/2/0	130048h	GTSP2_0_2_0_GTTMMADR	GT Scratch Pad 2
MMIO: 0/2/0	13004Ch	GTSP3_0_2_0_GTTMMADR	GT Scratch Pad 3
MMIO: 0/2/0	130050h	GTSP4_0_2_0_GTTMMADR	GT Scratch Pad 4
MMIO: 0/2/0	130054h	GTSP5_0_2_0_GTTMMADR	GT Scratch Pad 5
MMIO: 0/2/0	130058h	GTSP6_0_2_0_GTTMMADR	GT Scratch Pad 6
MMIO: 0/2/0	130090h	GTFORCEAWAKE_0_2_0_GTTMMADR	GT Force Awake