
# Intel® Open Source HD Graphics and Intel Iris™ Graphics

## Programmer's Reference Manual

For the 2014-2015 Intel Core™ Processors, Celeron™ Processors and Pentium™ Processors based on the "Broadwell" Platform

Volume 13: Memory-mapped Input/Output (MMIO)

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## Notices and Disclaimers

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# MMIO Shadow Table

Writes to the following registers from the CPU do not require force wake. Reads and writes from other sources do require force wake per the Force Wake Table section.

| Offset | Data (dw) | Source | Target Unit | Wake Domain | Description | Multiple cycle handling | Order |
|---|---|---|---|---|---|---|---|
| 0xA188 | 1 | IA | PM* | Force Wake | Replace data | Masked OR | 1 |
| 0xA270 | 1 | IA | PM | | Media Force Wake | Masked OR | 1 |
| 0xA278 | 1 | IA | PM | | Render Force Wake | Masked OR | 1 |
| 0xA008 | 1 | IA | PM | | RP normal request register | Replace data | 2 |
| 0xA00C | 1 | IA | PM | | RP video request register | Replace data | 2 |
| 0x2030 | 1 | IA | CS | Render | Tail Pointer | Replace data | 2 |
| 0x12030 | 1 | IA | VCS | Media | Tail Pointer | Replace data | 2 |
| 0x1C030 | 1 | IA | VCS2 | Media | Tail Pointer | Replace data | 2 |
| 0x22030 | 1 | IA | BCS | | Tail Pointer | Replace data | 2 |
| 0x1A030 | 1 | IA | VECS | Media | Tail Pointer | Replace data | 2 |
| 0x2230 | 8 | IA | CS | Render | Execlist submit FIFO | Replace oldest entry | 2 |
| 0x12230 | 8 | IA | VCS | Media | Execlist submit FIFO | Replace oldest entry | 2 |
| 0x22230 | 8 | IA | BCS | | Execlist submit FIFO | Replace oldest entry | 2 |
| 0x1C230 | 8 | IA | VCS2 | Media | Execlist submit FIFO | Replace oldest entry | 2 |
| 0x1A230 | 8 | IA | VECS | Media | Execlist submit FIFO | Replace oldest entry | 2 |
| 0x3800 | 1 | DE | CS | Render | Display->GT Messages multi-cast control CS | OR bits, clear on send to *CS | 4 |
| 0x23800 | 1 | DE | BCS | | Display->GT Messages multi-cast control BCS | OR bits, clear on send to *CS | 4 |
| 0x8508 | 1 | SA | MBC | | SA messages: DPR updates | OR bits, clear on send to *CS | 5 |
| 0x8500 | 1 | SA | MBC | | SA messages: VTd en/dis, invalidate Note: bit 12 is handled in a special duplicate register. See Aspec | OR bits, clear on send to *CS | 5 |
| 0x8100 | 1 | SA | CP | | SA messages: FLR | OR bits, clear on send to *CS | 6 |
| Any | 1 | IA | Any | Render | Driver selectable extra address | Replace data | 2 |
| Any | 1 | IA | Any | Media | Driver selectable extra address | Replace data | 2 |

| Offset | Data (dw) | Source | Target Unit | Wake Domain | Description | Multiple cycle handling | Order |
|---|---|---|---|---|---|---|---|
| Any | 1 | IA | Any | | IA->GT accesses | Replace data (NCU guarantees this can't happen) | 3 |
| Any | 1 | PCU | Any | | PCU->GT accesses | Replace data | 3 |
| 0x31000 | 4 | PCH | VCR | Media | Confirm KF1 (Boot time) | Replace data<br>Shadow not readable | 2 |
| 0x32130 | 4 | PCH | VCR | Media | Wireless key | Replace data<br>Shadow not readable | 2 |
| 0x31034 | 1 | IA or PCH | VCR | Media | Key/Session State Config | Replace data | 2 |
| 0x320FC | 1 | IA | VCR | Media | App ID (App init time) | Replace data | 2 |
| 0x32100 | 4 | PCH | VCR | Media | S1 key (App init time) | Replace data<br>Shadow not readable | 2 |
| 0x31020 | 4 | DE | VCR | Media | VCR1 Display port states – do not replicate | Replace data | 2 |
| 0x39020 | 4 | DE | VCR | Media | VCR2 Display port states – do not replicate | Replace data | 2 |
| | | | VCR2 | Media | Second VCR<br>Replicate from:<br>0x31xxx => 0x39xxx<br>0x32xxx => 0x3Axxx | | |
| 0x42A0 | 1 | SA | GAM | | SACOMMREG | Replace data | 5 |
| VT0x0C0 | 2 | IA | GAM | | Page Req Queue Head | Replace data | 2 |
| VT0x0C8 | 2 | IA | GAM | | Page Req Queue Tail | RO for IA, write by GAM to MGSR-range address (MMIO 0x0EC4, 0x0EC8) | 2 |
| VT0x0D0 | 2 | IA | GAM | | Page Req Queue Address | Replace data | 2 |
| VT0x100 | 2 | IA | GAM | | MTRR Capability | Replace data | 2 |
| VT0x108 | 2 | IA | GAM | | MTRR Default Type | Replace data | 2 |
| VT0x120 | 22 | IA | GAM | | IA32 MTRR FIX (range) | Replace data | 2 |
| VT0x180 | 40 | IA | GAM | | IA32 MTRR PHYS (range) | Replace data | 2 |
| 0x1400C | 1 | IA | WIN | | Reset Control Register | Replace data | 2 |
| 0x14030 | 1 | IA | WIN | | Target Frame size | Replace data | 2 |
| 0x14040 | 1 | DEProxy/IA | WIN | | Video Tail Pointer | Replace data | 3 |
| 0x1404C | 1 | DEProxy/IA | WIN | | Audio Tail pointer | Replace data | 2 |
| 0x14060 | 1 | DEProxy/IA | WIN | | TTL Timer | Replace data | 2 |
| 0x14064 | 1 | DEProxy/IA | WIN | | PCR 1 | | |

## Slice Registers and Die Recovery

When slice 0 is disabled (for example, GT3 fused to GT2 with a slice 0 fault), any read to a slice-located MMIO register must be directed to slice 1, otherwise data of '0' will be returned. This applies to SRM cycles from any command streamer.

| MMIO Range Start | MMIO Range End | Unit Description |
|---|---|---|
| 00005500 | 00005FFF | WMBE |
| 00007000 | 00007FFF | SVL |
| 00009400 | 000097FF | CP unit reg. file - Copy in Slice Common (in all slices) |
| 0000B000 | 0000B0FF | L3 unique status registers for each slice (unicast per GT). |
| 0000B100 | 0000B3FF | L3 bank config space (multicast copy per bank and slice) |
| 0000E000 | 0000E0FF | DM |
| 0000E100 | 0000E1FF | SC |
| 0000E200 | 0000E3FF | GWL (inst. 0) |
| 0000E200 | 0000E3FF | GWL (inst. 1) |
| 0000E200 | 0000E3FF | GWL (inst. 2) |
| 0000E400 | 0000E7FF | TDL |

# SW Virtualization Reserved MMIO range

The MMIO address range from 0x78000 thru 0x78FFF is reserved for communication between a VMM and the GPU Driver executing on a Virtual Machine.

HW does not actually implement anything within this range. Instead, in a SW Virtualized environment, if a VM driver issues a read to this MMIO address range, the VMM will trap that access, and provide whatever data it wishes to pass to the VM driver. In a non-SW-Virtualizated environment (including an SR-IOV Virtualized environment), reads will return zeros, like any other unimplemented MMIO address. Writes to this range are always ignored.

It is important that no "real" HW MMIO register be defined within this range, as it would be inaccessible in a SW-virtualized environment.