Intel® OpenSource HD Graphics Programmer's Reference Manual (PRM)

Volume 3 Part 3: PCH Display Registers (SandyBridge)

For the 2011 Intel Core Processor Family

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NOTICE:

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1. South Display Engine Registers [DevCPT]

1.1 Introduction

This chapter contains the register descriptions for the display portion of a family of graphics devices. These registers vary by devices within the family of devices, so special attention needs to be paid to which devices use which registers and register fields.

Different devices within the family may add, modify, or delete registers or register fields relative to another device in the same family based on the supported functions of that device.

1.1.1 Terminology

Description	Software Use	Should be implemented as
Read/Write, R/W	This bit can be read or written.	
Reserved	Don't assume a value for these bits. Writes have no effect.	Writes are ignored. Reads return zero.
Reserved: must be zero, MBZ	Software must always write a zero to these bits. This allows new features to be added using these bits that will be disabled when using old software and as the default case.	Writes are ignored. Reads return zero. Maybe be connected as Read/Write in future projects.
Reserved: PBC, software must preserve contents	Software must write the original value back to this bit. This allows new features to be added using these bits.	Read only.
Read Only	This bit is read only. The read value is determined by hardware. Writes to this bit have no effect.	According to each specific bit. The bit value is determined by hardware and not affected by register writes to the actual bit.
Read/Clear, Read/Write Clear	This bit can be read. Writes to it with a one cause the bit to clear.	Hardware events cause the bit to be set and the bit will be cleared on a write operation where the corresponding bit has a one for a value.
Double Buffered	Write when desired. Read gives the unbuffered value (written value) unless specified otherwise. Written values will update to take effect after a certain point. Some have a specific arming sequence where a write to another register is required before the update can take place. This is used to ensure atomic updates of several registers.	Two stages of registers used. First stage is written into and used for readback (unless specified otherwise). First stage value is transferred into second stage at the update point. Second stage value is used to control hardware. Arm/disarm flag for specific arming sequences.

1.1.2 Display Mode Set Sequence

See the North Display Engine Registers document.

1.1.3 Simultaneous Display Capabilities on a Single Display Pipe/Transcoder

	Embedded DP (on CPU)	Inte-grated LVDS	HDMI	DP	CRT
Embedded DP (on CPU)		No (7)	No (7)	No (7)	No (7)
Integrated LVDS			No (2, 3, 8)	No (2, 8,9)	No (3, 8)
HDMI			No(6, 8)	No(6, 8)	No (5, 8)
DP				No(3, 6, 8)	No (5, 8)
CRT					

Shading: Rose = Does not work, Yellow = Some cases work

1. No internal LVDS and HDMI, or DP on same pipe/transcoder.
2. No SSC on CRT, DVI, or HDMI. DP optionally has SSC.
3. Only works if DP/HDMI is in 24bpp mode.
4. Digital ports are multiplexed on the same pins, only works if ports are different.
5. Embedded DP is on the CPU; can not share the link.
6. Dithering, range correction, and gamma are done in the CPU; the display with lower bpp can truncate or the display with higher bpp can lose bits. One of the displays dictates range and gamma.
7. No DisplayPort allowed with other port on the same pipe/transcoder.
8. No HDMI allowed with another HDMI on the same transcoder.

1.1.4 Register Instances and Address Offsets

The main body of the register document only contains generic register format information.

The register offset spreadsheet gives the address of each register and which format it is an instance of.

2. South Shared Functions (C0000h–CFFFFh)

2.1 South Display Engine Interrupt Control Registers

2.1.1 South Display Engine Interrupt Bit Definition

South Display Engine Interrupt Bit Definition	
Project:	All
South Display Engine (SDE) interrupt bits come from events within the south display engine. The SDE_IIR bits are ORed together to generate the South/PCH Display Interrupt Event which will appear in the North Display Engine Interrupt Control Registers. Only the rising edge of the PCH Display interrupt will cause the North Display IIR (DEIIR) PCH Display Interrupt event bit to be set, so all PCH Display Interrupts, including back to back interrupts, must be cleared in the SDEIIR before a new PCH Display Interrupt can cause the DEIIR to be set. The South Display Engine Interrupt Control Registers all share the same bit definitions from this table.	
Bit	**Description**
31	**Audio_Power_State_change_Port_D** Project: All Format: This is an active high pulse when there is a power state change for audio for port D.
30	**Audio_Power_State_change_Port_C** Project: All Format: This is an active high pulse when there is a power state change for audio for port C.
29	**Audio_Power_State_change_Port_B** Project: All Format: This is an active high pulse when there is a power state change for audio for port B.
28	**Reserved** Project: All Format:
27	**AUX_Channel_D** Project: All Format: This is an active high pulse on the AUX D done event
26	**AUX_Channel_C** Project: All Format: This is an active high pulse on the AUX C done event
25	**AUX_Channel_B** Project: All Format: This is an active high pulse on the AUX B done event
24	**Reserved** Project: All Format:

South Display Engine Interrupt Bit Definition	
23	**DisplayPort/HDMI/DVI_D_Hotplug** Project: All Format: The ISR is an active high level representing the Digital Port D hotplug line when the Digital Port D hotplug detect input is enabled. The unmasked IIR is set on either a short or long pulse detection status in the Digital Port Hot Plug Control Register.
22	**DisplayPort/HDMI/DVI_C_Hotplug** Project: All Format: The ISR is an active high level representing the Digital Port C hotplug line when the Digital Port C hotplug detect input is enabled. The unmasked IIR is set on either a short or long pulse detection status in the Digital Port Hot Plug Control Register.
21	**DisplayPort/HDMI/DVI_B_Hotplug** Project: All Format: The ISR is an active high level representing the Digital Port B hotplug line when the Digital Port B hotplug detect input is enabled. The unmasked IIR is set on either a short or long pulse detection status in the Digital Port Hot Plug Control Register.
20	**Reserved** Project: All Format:
19	**CRT_Hotplug** Project: All Format: The ISR is an active high level representing the ORed together blue and green channel detection status as of the last detection cycle. The unmasked IIR is set on the rising or falling edges of the blue or green channel detection status in the Analog Port CRT DAC Control Register.
18	**Reserved** Project: All
17	**Gmbus** Project: All Format: This is an active high pulse when any of the events unmasked events in GMBUS4 Interrupt Mask register occur.
16	**Reserved** Project: All
15:11	**Reserved** Project: All Format:
10	**Audio_CP_Request_Transcoder_C** Project: All Format: This is an active high level indicating content protection is requested by audio azalia verb programming for transcoder C. It is valid after the Audio_CP_Change_Transcoder_C event has occurred.
9	**Audio_CP_Change_Transcoder_C** Project: All Format: This is an active high pulse when there is a change in the protection request from audio azalia verb programming for transcoder C.
8	**FDI_RX_Interrupts_Combined_C** Project: All Format: This is an active high level while any of the FDI_RX_ISR bits are set for transcoder C
7	**Reserved** Project: All Format:
6	**Audio_CP_Request_Transcoder_B** Project: All Format: This is an active high level indicating content protection is requested by audio azalia verb programming for transcoder B. It is valid after the Audio_CP_Change_Transcoder_B event has occurred.
5	**Audio_CP_Change_Transcoder_B** Project: All Format: This is an active high pulse when there is a change in the protection request from audio azalia verb programming for transcoder B.

South Display Engine Interrupt Bit Definition	
4	**FDI_RX_Interrupts_Combined_B** Project: All Format: This is an active high level while any of the FDI_RX_ISR bits are set for transcoder B
3	**Reserved** Project: All Format:
2	**Audio_CP_Request_Transcoder_A** Project: All Format: This is an active high level indicating content protection is requested by audio azalia verb programming for transcoder A. It is valid after the Audio_CP_Change_Transcoder_A event has occurred.
1	**Audio_CP_Change_Transcoder_A** Project: All Format: This is an active high pulse when there is a change in the protection request from audio azalia verb programming for transcoder A.
0	**FDI_RX_Interrupts_Combined_A** Project: All Format: This is an active high level while any of the FDI_RX_ISR bits are set for transcoder A

2.1.2 ISR — Interrupt Status

ISR

Register Type: MMIO
Project: All
Default Value: 00000000h
Access: Read Only
Size (in bits): 32

See the interrupt bit definition tables to find the source event for each interrupt bit.

Bit	Description
31:0	**Interrupt_Status_Bits** Project: All This field contains the non-persistent values of all interrupt status bits. The IMR register selects which of these interrupt conditions are reported in the persistent IIR.

Value	Name	Description	Project
0b	Condition Doesn't exist	Interrupt Condition currently does not exist	All
1b	Condition Exists	Interrupt Condition currently exists	All

Programming Notes
Some inputs to this register are short pulses; therefore software should not expect to use this register to sample these conditions.

2.1.3 IMR — Interrupt Mask

IMR

Register Type: MMIO
Project: All
Default Value: FFFFFFFFh
Access: R/W
Size (in bits): 32

See the interrupt bit definition tables to find the source event for each interrupt bit.

Bit	Description
31:0	**Interrupt_Mask_Bits** Project: All This field contains a bit mask which selects which interrupt bits from the ISR are reported in the IIR.

Value	Name	Description	Project
0b	Not Masked	Not Masked – will be reported in the IIR	All
1b	Masked	Masked – will not be reported in the IIR	All

2.1.4 IIR — Interrupt Identity

IIR	
Register Type:	MMIO
Project:	All
Default Value:	00000000h
Access:	R/W Clear
Size (in bits):	32

See the interrupt bit definition table to find the source event for each interrupt bit.

Bit	Description
31:0	**Interrupt_Identity_Bits** Project: All This field holds the persistent values of the interrupt bits from the ISR which are unmasked by the IMR. If enabled by the IER, bits set in this register will generate a PCH display interrupt. Bits set in this register will remain set (persist) until the interrupt condition is cleared by writing a '1' to the appropriate bits. For each bit, the IIR can store a second pending interrupt if two or more of the same interrupt conditions occur before the first condition is cleared. Upon clearing the interrupt, the IIR bit and PCH display interrupt will momentarily go low, then return high to indicate there is another interrupt pending. Only the rising edge of the PCH Display interrupt will cause the North Display IIR (DEIIR) PCH Display Interrupt event bit to be set, so all PCH Display Interrupts, including back to back interrupts, must be cleared here before a new PCH Display Interrupt can cause the DEIIR to be set.

Value	Name	Description	Project
0b	Condition Not Detected	Interrupt Condition Not Detected	All
1b	Condition Detected	Interrupt Condition Detected (may or may not have generated a PCH display interrupt)	All

2.1.5 IER — Interrupt Enable

IER	
Register Type:	MMIO
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

See the interrupt bit definition tables to find the source event for each interrupt bit.

Bit	Description
31:0	**Interrupt_Enable_Bits** Project: All The bits in this register enable a PCH display interrupt to be generated whenever the corresponding bit in the IIR becomes set. A disabled interrupt will still appear in the IIR register to allow polling of interrupt sources.

Value	Name	Description	Project
0b	Disable	Disable	All
1b	Enable	Enable	All

2.1.6 SHOTPLUG_CTL — South Hot Plug Control

SHOTPLUG_CTL	
Register Type:	MMIO
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

Bit	Description
31:21	**Reserved** Project: All Format:
20	**DP_D_HPD_Input_Enable** Project: All Default Value: 0b Controls the state of the HPD buffer for the digital port D. The buffer state is independent of whether the port is enabled or not.

Value	Name	Description	Project
0b	Disable	Buffer disabled	All
1b	Enable	Buffer enabled. Hot plugs bit reflect the electrical state of the HPD pin	All

SHOTPLUG_CTL

19:18 **DP_D_HPD_Short_Pulse_Duration**

Project: All

Default Value: 0b

These bits define the duration of the pulse defined as a short pulse for the digital port D.

Value	Name	Description	Project
00b	2ms	2mS	All
01b	4.5ms	4.5mS	All
10b	6ms	6mS	All
11b	100ms	100mS	All

17:16 **DP_D_HPD_Status**

Project: All

Default Value: 0b

This reflects hot plug detect status on the digital port D. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. When either a long or short pulse is detected, one of these bits will set. These bits are ORed together to go to the main ISR hotplug register bit.

Value	Name	Description	Project
00b	No Detect	Digital port hot plug event not detected	All
X1b	Short Detect	Digital port short pulse hot plug event detected	All
1Xb	Long Detect	Digital port long pulse hot plug event detected	All

15:13 **Reserved** Project: All Format:

12 **DP_C_HPD_Input_Enable**

Project: All

Default Value: 0b

Controls the state of the HPD buffer for the digital port C. The buffer state is independent of whether the port is enabled or not.

Value	Name	Description	Project
0b	Disable	Buffer disabled	All
1b	Enable	Buffer enabled. Hot plugs bit reflect the electrical state of the HPD pin	All

SHOTPLUG_CTL

11:10 **DP_C_HPD_Short_Pulse_Duration**

Project: All

Default Value: 0b

These bits define the duration of the pulse defined as a short pulse for the digital port C.

Value	Name	Description	Project
00b	2ms	2mS	All
01b	4.5ms	4.5mS	All
10b	6ms	6mS	All
11b	100ms	100mS	All

9:8 **DP_C_HPD_Status**

Project: All

Default Value: 0b

This reflects hot plug detect status on the digital port C. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. When either a long or short pulse is detected, one of these bits will set. These bits are ORed together to go to the main ISR hotplug register bit.

Value	Name	Description	Project
00b	No Detect	Digital port hot plug event not detected	All
X1b	Short Detect	Digital port short pulse hot plug event detected	All
1Xb	Long Detect	Digital port long pulse hot plug event detected	All

7:5 **Reserved** Project: All Format:

4 **DP_B_HPD_Input_Enable**

Project: All

Default Value: 0b

Controls the state of the HPD buffer for the digital port B. The buffer state is independent of whether the port is enabled or not.

Value	Name	Description	Project
0b	Disable	Buffer disabled	All
1b	Enable	Buffer enabled. Hot plugs bit reflect the electrical state of the HPD pin	All

SHOTPLUG_CTL	
3:2	**DP_B_HPD_Short_Pulse_Duration** Project: All Default Value: 0b These bits define the duration of the pulse defined as a short pulse for the digital port B.

Value	Name	Description	Project
00b	2ms	2mS	All
01b	4.5ms	4.5mS	All
10b	6ms	6mS	All
11b	100ms	100mS	All

1:0	**DP_B_HPD_Status** Project: All Default Value: 0b This reflects hot plug detect status on the digital port B. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug/unplug or for notification of a sink event. When either a long or short pulse is detected, one of these bits will set. These bits are ORed together to go to the main ISR hotplug register bit.

Value	Name	Description	Project
00b	No Detect	Digital port hot plug event not detected	All
X1b	Short Detect	Digital port short pulse hot plug event detected	All
1Xb	Long Detect	Digital port long pulse hot plug event detected	All

2.2 GMBUS and I/O Control Registers (C5000h–C5FFFh)

2.2.1 GPIO Pin Usage (By Functions)

GPIO pins allow the support of simple query and control functions such as DDC and I^2C interface protocols. GPIO pins exist in pairs (for the most part) and provide a mechanism to control external devices through a register programming interface. GPIO pins can be set to a level or the value of the pin can be read. This allows for a "bit banging" version of an I2C interface to be implemented. An additional function of using the GMBUS engine to run the I2C protocols is also allowed. Refer to the *CSpec* for GPIO signal descriptions. Refer to the *Philips I2C-BUS SPECIFICATION version 2.1* for a description of the I2C bus and protocol.

The number and names of the GPIO pins vary from device type to device type. Some of the GPIO pins will be muxed with other functions and are only available when the other function is not being used. The following subsections describe the GPIO pin to register mapping for the various devices. OEMs have the ability to remap these functions onto other pins as long as the hardware limitations are observed.

Port	Pin Use (Name)	GMBUS Use	Internal Pullup	I^2C	Device	Description
5	HDMI/DPD CTLDATA	Yes	No (weak pulldown on reset)	Yes	All	DDC for HDMI connection via the integrated HDMI port D
	HDMI/DPD CTLCLK		No	Yes		
4	HDMIB CTLDATA	Yes	No (weak pulldown on reset)	Yes	All	Used for programming HDMI device via GMBUS protocol.
	HDMIB CTLCLK		No	Yes		
3	HDMI/DPC CTLDATA	Yes	No (weak pulldown on reset)	Yes	All	DDC for HDMI connection via the integrated HDMI port C.
	HDMI/DPC CTLCLK		No	Yes		
2	LVDS DDC Data (DDCLDATA)	Yes	No	Yes	All	DDC for Digital Display connection via the integrated LVDS
	LVDS DDC Clock (DDCLCLK)			Yes		
1	I2C Data (LCLKCTRLB)	Yes	No	Yes	All	For control of SSC clock generator devices on motherboard. Support can be optionally I2C or control level.
	I2C Clock (LCLKCTRLA)			Yes		
0	DAC DDC Data (DDCADATA)	Yes	No	Yes	All	DDC for Analog monitor (VGA) connection. This cannot be shared with other DDC or I2C pairs due to legacy monitor issues.
	DAC DDC Clock (DDCACLK)			Yes		

2.2.2 GPIO_CTL –GPIO Control

GPIO Control Register Format

Project: All

Bit	Description
31:13	**Reserved** Project: All Format: MBZ
12	**GPIO_Data_In** Project: All Access: Read Only This is the value that is sampled on the GPIO_Data pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset.
11	**GPIO_Data_Value** Project: All Access: R/W Default Value: 1b This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if **GPIO DATA MASK** is also asserted. The value will appear on the pin if this data value is actually written to this register and the **GPIO Data DIRECTION VALUE** contains a value that will configure the pin as an output. **Default = 1.** The GPIO default clock data value is programmed to '1' in hardware. The hardware drives a default of '1' since the I2C interface defaults to a '1'. (this mimics the I2C external pull-ups on the bus)
10	**GPIO_Data_Mask** Project: All Access: Write Only Default Value: 0b This is a mask bit to determine whether the **GPIO DATA VALUE** bit should be written into the register. This value is not stored and when read returns 0.

Value	Name	Description	Project
0b	No Write	Do NOT write GPIO Data Value bit	All
1b	Write	Write GPIO Data Value bit.	All

9	**GPIO_Data_Direction_Value** Project: All Access: R/W Default Value: 0b This is the value that should be used to define the output enable of the GPIO Data pin. This value is only written into the register if **GPIO Data DIRECTION MASK** is also asserted. The value that will appear on the pin is defined by what is in the register for the **GPIO DATA VALUE** bit.

Value	Name	Description	Project
0b	Input	Pin is configured as an input	All
1b	Output	Pin is configured as an output	All

GPIO Control Register Format

8	**GPIO_Data_Direction_Mask** Project: All Access: Write Only Default Value: 0b This is a mask bit to determine whether the **GPIO DIRECTION VALUE** bit should be written into the register. This value is not stored and when read always returns 0.

Value	Name	Description	Project
0b	No Write	Do NOT write GPIO Data Direction Value bit	All
1b	Write	Write GPIO Data Direction Value bit	All

7:5	**Reserved** Project: All Format: MBZ
4	**GPIO_Clock_Data_In** Project: All Access: Read Only This is the value that is sampled on the GPIO Clock pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input, this bit is undefined at reset.
3	**GPIO_Clock_Data_Value** Project: All Access: R/W Default Value: 1b This is the value that should be place on the GPIO Clk pin as an output. This value is only written into the register if **GPIO Clock DATA MASK** is also asserted. The value will appear on the pin if this data value is actually written to this register and the **GPIO Clock DIRECTION VALUE** contains a value that will configure the pin as an output. **Default = 1.** The GPIO default clock data value is programmed to '1' in hardware. The hardware drives a default of '1' since the I2C interface defaults to a '1'. (this mimics the I2C external pull-ups on the bus)
2	**GPIO_Clock_Data_Mask** Project: All Access: Write Only Default Value: 0b This is a mask bit to determine whether the **GPIO Clock DATA VALUE** bit should be written into the register. This value is not stored and when read always returns 0.

Value	Name	Description	Project
0b	No Write	Do NOT write GPIO Clock Data Value bit	All
1b	Write	Write GPIO Clock Data Value bit	All

GPIO Control Register Format

1	**GPIO_Clock _Direction_Value** Project: All Access: R/W Default Value: 0b This is the value that should be used to define the output enable of the GPIO Clock pin. This value is only written into the register if **GPIO Clock DIRECTION MASK** is also asserted. The value that will appear on the pin is defined by what is in the register for the **GPIO Clock DATA VALUE** bit.

Value	Name	Description	Project
0b	Input	Pin is configured as an input and the output driver is set to tri-state	All
1b	Output	Pin is configured as an output	All

0	**GPIO_Clock_Direction_Mask** Project: All Access: Write Only Default Value: 0b This is a mask bit to determine whether the **GPIO Clock DIRECTION VALUE** bit should be written into the register. This value is not stored and when read returns 0.

Value	Name	Description	Project
0b	No Update	Do NOT update the GPIO Clock Direction Value bit on a write	All
1b	Update	Update the GPIO Clock Direction Value bit. on a write operation to this register	All

GPIO_CTL

Register Type: MMIO
Project: All
Default Value: 000U1000b
Access: R/W
Size (in bits): 6x32

These registers define the control of sets of the “general purpose” I/O pins. Each register controls a pair of pins that can be used for general purpose control, but most are designated for specific functions according to the requirements of the device and the system that the device is in. Each pin of the two pin pair is designated as a clock or data for descriptive purposes. See the table at the beginning of this section to determine which pins/registers are supported and their intended functions. **Board design variations are possible and would affect the usage of these pins.**

The registers that control digital display (HDMI/DVI, DisplayPort) pins should only be utilized if the Port Detected bit in the related control register is set to 1.

DWord	Bit	Description
0	31:0	GPIOCTL_0 Project: All Format: GPIO Control Register Format

GPIO_CTL						
1	31:0	GPIOCTL_1	Project:	All	Format:	GPIO Control Register Format
2	31:0	GPIOCTL_2	Project:	All	Format:	GPIO Control Register Format
3	31:0	GPIOCTL_3	Project:	All	Format:	GPIO Control Register Format
4	31:0	GPIOCTL_4	Project:	All	Format:	GPIO Control Register Format
5	31:0	GPIOCTL_5	Project:	All	Format:	GPIO Control Register Format

2.2.3 GMBUS Controller Programming Interface

The GMBUS (Graphic Management Bus) can be used to indirectly access/control devices connected to a GMBUS bus as an alternate to bit-wise programming via software.

The GMBUS interface is I^2C compatible. The basic features are listed as follow:

1. Works as the master of a single master bus.
2. The bus clock frequency is selectable by software to be 50KHz, 100KHz, 400KHz , and 1MHz
3. The GMBUS controller can be attached to the selected GPIO pin pairs.
4. 7 or 10-Bit Slave Address and 8- or 16-bit index.
5. Hardware byte counter to track the data transmissions/reception
6. Timing source from core display clock.
7. There is a double buffered data register and a 9 bit counter to support 0 byte to 256 byte transfers.
8. The slave device can cause a stall by pulling down the clock line (Slave Stall), or delay the slave acknowledge response.
9. The master controller detects and reports time out conditions for a stall from a slave device or delayed or missing slave acknowledge.
10. Interrupt may optionally be generated.
11. There is no support for ring buffer based operation of GMBUS. The GMBUS is controlled by a set of memory mapped IO registers. Status is reported through the GMBUS status register.
12. GMBUS does not directly support segment pointer addressing as defined by the Enhanced Display Data Channel standard. Segment pointer addressing for EDDC shall be supported as follows:

a. Use bit bashing (GPIO programming) to complete segment pointer register write over the target I2C port **without terminating in a stop or wait cycle**.

b. Terminate bit bashing phase with both I2C lines pulled high by tri-stating the data line before the clock line. Follow EDDC requirement for response received from slave device.

c. Initiate gmbus cycle as required to transfer EDID follow normal procedure.

The byte counter register is a read/write register, and in receiving mode, is used to track the data bytes received. There is a status register to indicate the error condition, data buffer busy, time out, and data complete acknowledgement.

2.2.3.1 GMBUS0—GMBUS Clock/Port Select

GMBUS0—GMBUS Clock/Port Select

Register Type: MMIO
Address Offset: C5100h
Project: All
Default Value: 00000000h
Access: R/W
Size (in bits): 32

The GMBUS0 register will set the clock rate of the serial bus and the device the controller is connected to. The clock rate options are 50 KHz, 100 KHz, 400 KHz, and 1MHz. This register should be set before the first data valid bit is set, because it will be read only at the very first data valid bit, and not read during the period of the transmission until stop is issued and next first data valid bit is set.

Bit	Description
31:12	**Reserved** Project: All Format:
11	**Reserved**
10:8	**GMBUS_Rate_Select** Project: All Default Value: 0b These two bits select the rate that the GMBUS will run at. It also defines the AC timing parameters used. It should only be changed when between transfers when the GMBUS is idle.
7:3	**Reserved** Project: All Format: MBZ

Value	Name	Description	Project
000b	100KHz	100 KHz	All
001b	50KHz	50 KHz	All
010b	400KHz	400 KHz	All
1XXb	RESERVED	Reserved	All

GMBUS0—GMBUS Clock/Port Select

2:0 **Pin_Pair_Select**

Project: All

Default Value: 0b

This field selects a GMBUS pin pair for use in the GMBUS communication. Use the table above to determine which pin pairs are available for a particular device and the intended function of that pin pair. Note that it is not a straight forward mapping of port numbers to pair select numbers.

Value	Name	Description	Project
000b	None	None (disabled)	All
001b	LCTRCLK	LCTRCLKA, LCTRLCLKB SSC Clock Device	All
010b	Analog Mon	Dedicated Analog Monitor DDC Pins (DDC1DATA, DDC1CLK)	All
011b	LVDS	Integrated Digital Panel DDC Pins, LVDS	All
100b	Port C	DP/HDMI port C Use	All
110b	Port D	DP/HDMI port D Use	All
111b	Reserved	Reserved	All

2.2.3.2 GMBUS1—GMBUS Command/Status

GMBUS1—GMBUS Command/Status

Register Type: MMIO
Address Offset: C5104h
Project: All
Default Value: 00000000h
Access: R/W Protect
Size (in bits): 32

This register lets the software indicate to the GMBUS controller the slave device address, register index, and indicate when the data write is complete.

When the SW_CLR_INT bit is asserted, all writes to the GMBUS2, GMBUS3, and GMBUS4 registers are discarded. The GMBUS1 register writes to any other bit except the SW_CLR_INT are also lost. Reads to these registers always work normally regardless of the state of the SW_CLR_INT bit.

Bit	Description
31	**Software_Clear_Interrupt** Project: All Access: R/W Default Value: 0b (SW_CLR_INT) This bit must be clear for normal operation. Setting the bit then clearing it acts as local reset to the GMBUS controller. This bit is commonly used by software to clear a BUS_ERROR when a slave device delivers a NACK.
30	**Software_Ready** Project: All Default Value: 0b (SW_RDY) Data handshake bit used in conjunction with **HW_RDY** bit.

Bit 31 — Software_Clear_Interrupt

Value	Name	Description	Project
0b	Clear HW_RDY	If this bit is written as a zero when its current state is a one, will clear the **HW_RDY** bit and allows register writes to be accepted to the GMBUS registers (Write Protect Off). This bit is cleared to zero when an event causes the HW_RDY bit transition to occur.	All
1b	Assert HW_RDY	Asserted by software after servicing the GMBUS interrupt. Setting this bit causes the INT status bit to be cleared. Setting (1) this bit also asserts the **HW_RDY** bit (until this bit is written with a 0). When this bit is set, no writes to GMBUS registers will cause the contents to change with the exception of this bit which can be written.	All

Bit 30 — Software_Ready

Value	Name	Description	Project
0b	De-Assert	De-asserted via the assertion event for **HW_RDY** bit	All
1b	SW Assert	When asserted by software, results in de-assertion of **HW_RDY** bit	All

GMBUS1—GMBUS Command/Status

29 **Enable_Timeout**

Project: All

Default Value: 0b

(ENT) Enables timeout for slave response. When this bit is enabled and the slave device response has exceeded the timeout period, the GMBUS Slave Stall Timeout Error interrupt bit is set.

Value	Name	Description	Project
0b	Disable	Disable timeout counter	All
1b	Enable	Enable timeout counter	All

28 **Reserved** Project: All Format:

27:25 **Bus_Cycle_Select**

Project: All

Default Value: 0b

GMBUS cycle will always consist of a START followed by Slave Address, followed by an optional read or write data phase. A read cycle with an index will consist of a START followed by a Slave Address a WRITE indication and the INDEX and then a RESTART with a Slave Address and an optional read data phase. The GMBUS cycle will terminate either with a STOP or by entering a wait state. The WAIT state is exited by generating a STOP or by starting another GMBUS cycle.

This can only cause a STOP to be generated if a GMBUS cycle is generated, the GMBUS is currently in a data phase, or it is in a WAIT phase:

Note that the three bits can be decoded as follows:

27 = STOP generated

26 = INDEX used

25 = Cycle ends in a WAIT

Value	Name	Description	Project
000b	No cycle	No GMBUS cycle is generated	All
001b	No Index, No Stop, Wait	GMBUS cycle is generated without an INDEX, with no STOP, and ends with a WAIT	All
010b	Reserved	Reserved	All
011b	Index, No Stop, Wait	GMBUS cycle is generated with an INDEX, with no STOP, and ends with a WAIT	All
100b	Gen Stop	Generates a STOP if currently in a WAIT or after the completion of the current byte if active	All
101b	No Index, Stop	GMBUS cycle is generated without an INDEX and with a STOP	All
110b	Reserved	Reserved	All
111b	Index, Stop	GMBUS cycle is generated with an INDEX and with a STOP	All

24:16 **Total_Byte_Count** Project: All Format:

(9-bits) This determines the total number of bytes to be transferred during the DATA phase of a GMBUS cycle. The DATA phase can be prematurely terminated by generating a STOP while in the DATA phase (see Bus Cycle Select). Do not change the value of this field during GMBUS cycles transactions.

GMBUS1—GMBUS Command/Status

15:8	**8_bit_Slave_Register_Index** Project: All Format: (INDEX) This field specifies the 8-bits of index to be used for the generated bus write transaction or the index used for the WRITE portion of the WRITE/READ pair. It only has an effect if the enable Index bit is set. Do not change this field during a GMBUS transaction.
7:0	**Slave_Address_And_Direction** Project: All Bits 7:1 = **7-bit GMBUS Slave Address (SADDR):** When a GMBUS cycle is to be generated using the Bus Cycle Select field, this field specifies the value of the slave address that is to be sent out. For use with 10-bit slave address devices, set this value to 11110XXb (where the last two bits (xx) are the two MSBs of the 10-bit address) and the slave direction bit to a write. This is followed by the first data byte being the 8 LSBs of the 10-bit slave address. Bit 0 = **Slave Direction Bit:** When a GMBUS cycle is to be generated based on the Bus Cycle Select, this bit determines if the operation will be a read or a write. A read operation with the index enabled will perform a write with just the index followed by a re-start and a read. A 1 indicates that a Read from the slave device operation is to be performed. A 0 indicates that a Write to the slave device operation is to be performed.

Value	Name	Description	Project
00000001b	General	General Call Address	All
00000000b	Start	Start Bye	All
0000001Xb	CBUS	CBUS Address	All
11110XXXb	10-bit	10-Bit addressing	All
Others	Reserved	Reserved	All

2.2.3.3 GMBUS2—GMBUS Status Register

GMBUS2—GMBUS Status Register

Register Type: MMIO
Address Offset: C5108h
Project: All
Default Value: 00000800h
Access: R/W Protect
Size (in bits): 32

Bit	Description
31:16	**Reserved** Project: All Format:
15	**INUSE** Project: All Default Value: 0b Software wishing to arbitrate for the GMBUS resource can poll this bit until it reads a zero and will then own usage of the GMBUS controller. This bit has no effect on the hardware, and is only used as semaphore among various independent software threads that don't know how to synchronize their use of this resource that may need to use the GMBUS logic. Writing a one to this bit is software's indication that the software use of this resource is now terminated and it is available for other clients.
14	**Hardware_Wait_Phase** Project: All Access: Read Only Default Value: 0b **(HW_WAIT_PHASE)** Once in a WAIT_PHASE, the software can now choose to generate a STOP cycle or a repeated start (RESTART) cycle followed by another GMBUS transaction on the GMBUS.

Value	Name	Description	Project
0b	GMBUS is Acquired	Read operation that contains a zero in this bit position indicates that the GMBUS engine is now acquired and the subsequent reads of this register will now have this bit set. Writing a 0 to this bit has no effect.	All
1b	GMBUS in Use	Read operation that contains a one for this bit indicates that the GMBUS is currently allocated to someone else and "In use". Once set, a write of a 1 to this bit indicates that the software has relinquished the GMBUS resource and will reset the value of this bit to a 0.	All

Value	Name	Description	Project
0b	No Wait	The GMBUS engine is not in a wait phase.	All
1b	Wait	Set when GMBUS engine is in wait phase. Wait phase is entered at the end of the current transaction when that transaction is selected not to terminate with a STOP.	All

GMBUS2—GMBUS Status Register

13

Slave_Stall_Timeout_Error

Project: All

Access: Read Only

Default Value: 0b

This bit indicates that a slave stall timeout has occurred. It is tied to the Enable Timeout (ENT) bit.

Value	Name	Description	Project
0b	No Slave Timeout	No slave timeout has occurred	All
1b	Slave Timeout	A slave acknowledge timeout has occurred	All

12

GMBUS_Interrupt_Status

Project: All

Access: Read Only

Default Value: 0b

This bit indicates that an event that causes a GMBUS interrupt has occurred.

Value	Name	Description	Project
0b	No Interrupt	The conditions that could cause a GMBUS interrupt have not occurred or this bit has been cleared by software assertion of the **SW_CLR_INT** bit.	All
1b	Interrupt	GMBUS interrupt event occurred. This interrupt must have been one of the types enabled in the GMBUS4 register	All

GMBUS2—GMBUS Status Register

11 **Hardware_Ready**

Project: All

Access: Read Only

Default Value: 1b See Description Below

(HW_RDY) This provides a method of detecting when the current software client routine can proceed with the next step in a sequence of GMBUS operations. This data handshake bit is used in conjunction with the **SW_RDY** bit. When this bit is asserted by the GMBUS controller, it results in the de-assertion of the **SW_RDY** bit.

This bit resumes to normal operation when the **SW_CLR_INT** bit is written to a 0.

Value	Name	Description	Project
0b		Condition required for assertion has not occurred or when this bit is a one and: - **SW_RDY** bit has been asserted - During a GMBUS read transaction, after the each read of the data register - During a GMBUS write transaction, after each write of the data register - **SW_CLR_INT** bit has been cleared	All
1b		This bit is asserted under the following conditions: - After a reset or when the transaction is aborted by the setting of the **SW_CLR_INT** bit - When an active GMBUS cycle has terminated with a STOP - When during a GMBUS write transaction, the data register needs and can accept another four bytes of data - During a GMBUS read transaction, this bit is asserted when the data register has four bytes of new data or the read transaction DATA phase is complete and the data register contains the last few bytes of the read data	All

10 **NAK_Indicator**

Project: All

Access: Read Only

Default Value: 0b

Value	Name	Description	Project
0b	No bus error	No bus error has been detected or **SW_CLR_INT** has been written as a zero since the last bus error	All
1b	No Ack	Set by hardware if any expected device acknowledge is not received from the slave within the timeout	All

GMBUS2—GMBUS Status Register	
9	**GMBUS_Active** Project: All Access: Read Only Default Value: 0b **(GA)** This is a status bit that indicates whether the GMBUS controller is in an IDLE state or not. **Value** / **Name** / **Description** / **Project** 0b / Idle / The GMBUS controller is currently IDLE / All 1b / Active / This indicates that the bus is in START, ADDRESS, INDEX, DATA, WAIT, or STOP Phase. Set when GMBUS hardware is not IDLE. / All
8:0	**Current_Byte_Count** Project: All Access: Read Only Can be used to determine the number of bytes currently transmitted/received by the GMBUS controller hardware. Set to zero at the start of a GMBUS transaction data transfer and incremented after the completion of each byte of the data phase. Note that because reads have internal storage, the byte count on a read operation may be ahead of the data that has been accepted from the data register.

2.2.3.4 GMBUS3—GMBUS Data Buffer

GMBUS3—GMBUS Data Buffer				
Register Type:	MMIO			
Address Offset:	C510Ch			
Project:	All			
Default Value:	00000000h			
Access:	R/W Protect			
Size (in bits):	32			
Double Buffer Update Point:	Start of next Vblank			
Double Buffer Armed By:	HW_RDY			
This is data read/write register. This register is double buffered. Bit 0 is the first bit sent or read, bit 7 is the 8th bit sent or read, all the way through bit 31 being the 32nd bit sent or read. For GMBUS write operations with a non-zero byte count, this register should be written with the data before the GMBUS cycle is initiated. For byte counts that are greater than four bytes, this register will be written with subsequent data only after the HW_RDY status bit is set indicating that the register is now ready for additional data. For GMBUS read operations, software should wait until the HW_RDY bit indicates that the register contains the next set of valid read data before reading this register.				
Bit	**Description**			
31:24	**Data Byte 3**	Project:	All	Format:
23:16	**Data Byte 2**	Project:	All	Format:
15:8	**Data Byte 1**	Project:	All	Format:
7:0	**Data Byte 0**	Project:	All	Format:

2.2.3.5 GMBUS4—GMBUS Interrupt Mask

GMBUS4—GMBUS Interrupt Mask

Register Type: MMIO
Address Offset: C5110h
Project: All
Default Value: 00000000h
Access: R/W
Size (in bits): 32

Bit	Description
31:5	**Reserved** Project: All Format:
4:0	**Interrupt_Mask** Project: All Default Value: 0b This field specifies which GMBUS interrupts events may contribute to the setting of GMBUS interrupt status bit in second level interrupt status register.

Value	Name	Description	Project
0XXXXb	GMBUS Slave stall TO Disable	Disable GMBUS Slave stall timeout interrupt	All
1XXXXb	GMBUS Slave stall TO Enable	Enable GMBUS Slave stall timeout interrupt	All
X0XXXb	GMBUS NAK Disable	Disable GMBUS NAK interrupt	All
X1XXXb	GMBUS NAK Enable	Enable GMBUS NAK interrupt	All
XX0XXb	GMBUS Idle Disable	Disable GMBUS Idle interrupt	All
XX1XXb	GMBUS Idle Enable	Enable GMBUS Idle interrupt	All
XXX0Xb	HW Wait Disable	Disable Hardware wait (GMBUS cycle without a stop has completed) Interrupt	All
XXX1Xb	HW Wait Enable	Enable Hardware wait (GMBUS cycle without a stop has completed) Interrupt	All
XXXX0b	HW Ready Disable	Disable Hardware ready (Data has been transferred) interrupt	All
XXXX1b	HW Ready Enable	Enable Hardware ready (Data has been transferred) interrupt	

2.2.3.6 GMBUS5—GMBUS 2 Byte Index Register

GMBUS5—GMBUS 2 Byte Index Register	
Register Type:	MMIO
Address Offset:	C5120h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

This register provides a method for the software indicate to the GMBUS controller the 2 byte device index.

Bit	Description
31	**2_Byte_Index_Enable** Project: All Format: When this bit is asserted (1), then bits 15:0 are used as the index. Bits 15:8 are used in the first byte which is the most significant index bits. The slave index in the GMBUS1<15:8> are ignored. Bits 7:0 are used in the second byte which is the least significant index bits.
30:16	**Reserved** Project: All Format:
15:0	**2_Byte_Slave_Index** Project: All Format: This is the 2 byte index used in all GMBUS accesses when bit 31 is asserted (1).

2.3 Display Clock Control Registers (C6000h–C6FFFH)

Pixel Data Rate	Dot Clock	Dual Channel?	External Clock	Data Clock Rate	Multiplier
HDMI 25-50MHz	100-200MHz	NO	100-200MHz	1.0-2.0GHz	4x
HDMI 50-100MHz	100-200MHz	NO	100-200MHz	1.0-2.0GHz	2x
HDMI 100-225MHz	100-225MHz	NO	100-225MHz	1.0-2.25GHz	1x
LVDS 25-112MHz	25-112MHz	NO	25-112MHz	175-784MHz	1x
LVDS 80-224MHz	80-224MHz	YES	80-224MHz	280-784MHz	1x

Display Modes	Display Clock Frequency Range (MHz)
CRT DAC	25-350
HDMI	25-225 (pixel rate can differ from clock frequency)
LVDS (Single Channel)	25-112

Display Modes	Display Clock Frequency Range (MHz)
LVDS (Dual Channel)	80-224
Display Port	162, 270 (pixel rate can differ from clock frequency)

The PLL frequency selection must be done such that the internal VCO frequency is within its limits. The PLL Frequency is based on the selected register and the following formula. The post divider register value limits are different for LVDS mode.

Reference Frequency: 120MHz for CRT, HDMI, LVDS. 100MHz for the FDI.

DotClk_Frequency = (ReferenceFrequency * (5* (M1+2)+(M2+2)) / (N+2))/ (P1* P2)

Item	Units	Range	Notes
Dot Clock	Frequency	20-350	MHz (Combining ALL modes)
VCO	Frequency	1760-3510	MHz
N – Counter	Value	3-8	
M – Counter	Value	79-127	M=5*(M1+2)+(M2+2)
M1 and M2		M1 > M2	
M1	Value	12-22	
M2	Value	5-9	
P-Div	Value	5-80	Combined P1 and P2 for DAC mode
P-Div	Value	28-112	Combined P1 and P2 for LVDS mode
P1-Div	Value	1-8	All modes

Note: For HDMI 12bpc usage model, the PCH display pixel clock should be programmed at 1.5x the effective pixel clock of the CPU display. This needs to be taken into account when setting the post divisors.

2.3.1 DPLL_CTL—DPLL Control

DPLL_CTL	
Register Type:	MMIO
Project:	All
Default Value:	04800080h
Access:	R/W Protect
Size (in bits):	32
Double Buffer Update Point:	Transcoder vertical blank, except as stated

Write Protect by Panel Power Sequencer when panel is connected to this transcoder.

Bit	Description
31	**DPLL_VCO_Enable** Project: All Access: R/W Default Value: 0b This bit will enable or disable the PLL VCO. Disabling the PLL will cause the display clock to stop.

Value	Name	Description	Project
0b	Disable	DPLL is disabled in its lowest power state	All
1b	Enable	DPLL is enabled and operational	All

Bit	Description
30	**DPLL_High_Speed_IO_clock_En** Project: All Default Value: 0b

Value	Name	Description	Project
0b	Disable	High Speed IO Clock Disabled	All
1b	Enable	High Speed IO Clock Enabled (must be set in HDMI, and DisplayPort modes)	All

Bit	Description
29:28	**Reserved** Project: All Format: MBZ
27:26	**DPLL_Mode_Select** Project: All Default Value: 01b Non-LVDS Configure the DPLL for various supported Display Modes

Value	Name	Description	Project
00b	Reserved	Reserved	All
01b	Non-LVDS	DPLL in DAC/HDMI/DisplayPort mode (default)	All
10b	LVDS	DPLL in LVDS mode	All
11b	Reserved	Reserved	All

DPLL_CTL

25:24 **FP0_FP1_P2_Clock_Divide**

Project: All

Default Value: 00b

Value	Name	Description	Project
00b	Div 14_10	Divide by 14 for Single-Channel LVDS Divide by 10 for DisplayPort. Also used for DAC and HDMI modes with Dot Clock <= 225MHz	All
01b	Div 7_5	Divide by 7 for Dual-Channel LVDS Divide by 5 for DAC and HDMI modes with Dot Clock > 225MHz	All
Others	Reserved	Reserved	All

23:16 **FP0_P1_Post_Divisor**

Project: All

Default Value: 80h Divide by eight

Writes to this byte finalize the write of m, n and p values into the PLL when the PLL is disabled. Writing to FP1 when FP0 is in use (or vice versa) is also allowed. **Writes to this register take effect immediately.**

Value	Name	Description	Project
00000001b	1	Divide by one	All
00000010b	2	Divide by two	All
00000100b	3	Divide by three	All
00001000b	4	Divide by four	All
00010000b	5	Divide by five	All
00100000b	6	Divide by six	All
01000000b	7	Divide by seven	All
10000000b	8	Divide by eight (default)	All
Others	Reserved	Reserved	All

DPLL_CTL

15:13 **PLL_Reference_Input_Select**

Project: All

Default Value: 000b

(Not Double Buffered) The PLL reference should be selected based on the display device that is being driven. The standard reference clock is used for CRT modes using the analog port CRT DAC or LCD panels for the integrated LVDS.

Value	Name	Description	Project
000b	DREFCLK	DREFCLK (default is 120 MHz) for DAC/HDMI/DVI/DisplayPort	All
001b	Super SSC	120MHz super-spread clock	All
011b	SSC	Spread spectrum input clock (120MHz default) for LVDS/DisplayPort	All
Others	Reserved	Reserved	All

12 **Reserved** Project: All Format:

11:9 **DPLL_ HDMI_multiplier**

Project: All

Default Value: 000b (1X)

Range 0..3

In order to keep the clock rate to a more narrow range of rates, the multiplier is set and the Display PLL programmed to a multiple of the display mode's actual clock rate. The DPLL must be enabled and stable before setting these bits. These bits must be programmed after DPLL_SEL is programmed

Value in this register = multiplication factor - 1

8 **Reserved** Project: All Format: MBZ

DPLL_CTL	
7:0	**FP1_P1_Post_Divisor** Project: All Default Value: 80h Divide by eight Writes to this byte finalize the write of m, n and p values into the PLL when the PLL is disabled. Writing to FP1 when FP0 is in use (or vice versa) is also allowed. Writes to this register take effect immediately.

Value	Name	Description	Project
00000001b	1	Divide by one	All
00000010b	2	Divide by two	All
00000100b	3	Divide by three	All
00001000b	4	Divide by four	All
00010000b	5	Divide by five	All
00100000b	6	Divide by six	All
01000000b	7	Divide by seven	All
10000000b	8	Divide by eight (Default)	All
Others	Reserved	Reserved	All

2.3.2 DPLL_FP0—DPLL Divisor 0

DPLL_FP0	
Register Type:	MMIO
Project:	All
Default Value:	00030D07h
Access:	R/W Protect
Size (in bits):	32
Double Buffer Update Point:	Transcoder vertical blank
Write Protect by Panel Power Sequencer when panel is connected to this transcoder.	

Bit	Description
31:28	**Reserved** Project: All Format: MBZ
27	**Frequency_doubler_clock_enable** Project: All Default Value: 0b This bit enables/disables the frequency doubler clock. When the VCO clock to the doubler is disabled, the circuit does not dissipate power and its output clock is not available

Value	Name	Description	Project
0b	Disable	Disables clock of frequency doubler	All
1b	Enable	Enables clock of frequency doubler	All

DPLL_FP0

26:25	**Reserved** Project: All Format: MBZ
24:22	**CB_Tuning** Project: All Default Value: 000b These bits are used for CB tuning the Display PLL Analog core on PCH. These bits are required to improve the jitter performance and VCO headroom of the Display PLL across Process, Voltage and Temperature variations. The CB tune should be turned on when the M/N ratio is less than a certain value given in the table below. The bits should be programmed to 0x011 to turn the complete CB cap on.

Display Mode	If M/N Ratio is less than	Bits <24:22>
DAC	21.00	011
HDMI	21.00	011
LVDS 1ch (120mhz input clock)	21.00	011
LVDS 2ch (120mhz input clock)	25.00	011
LVDS 1ch (100mhz input clock)	25.00	011
LVDS 2ch (100mhz input clock)	25.00	011

Example1:

In DAC mode, for pixel clock = 31MHz, N=4; M=83; P=80;

Therefore M/N ratio = 20.75 which is < 21.00 mentioned in the table above. Hence the CB tune bits <24:22> need to be programmed to 011.

Example2:

In DAC mode, for pixel clock = 31.5MHz, N=4; M=84; P=80;

Therefore M/N ratio = 21 which equal to the value of M/N ration mentioned in the table above. Hence the CB tune bits <24:22> need to be programmed to 000.

Value	Name	Description	Project
000b	Off	CB Tune Off	All
011b	100%	CB Tune 100% On	All

21:16	**FP0_N_Divisor** Project: All Format: N-Divisor value calculated for the desired output frequency. The register value is programmed two less than the actual divisor.
15:14	**Reserved** Project: All Format: MBZ

DPLL_FP0	
13:8	**FP0_M1_Divisor** Project: All Format: M-Divisor value calculated for the desired output frequency. The register value is programmed to two less than the actual divisor.
7:6	**Reserved** Project: All Format: MBZ
5:0	**FP0_M2_Divisor** Project: All Format: M-Divisor value calculated for the desired output frequency. The register value is programmed two less than the actual divisor.

2.3.3 DPLL_FP1—DPLL Divisor 1

DPLL_FP1

Register Type: MMIO
Project: All
Default Value: 00030D07h
Access: R/W Protect
Size (in bits): 32
Double Buffer Update Point: Transcoder vertical blank
Write Protect by Panel Power Sequencer when panel is connected to this transcoder.

Bit	Description
31:25	**Reserved** Project: All Format: MBZ
24:22	**CB_Tuning** Project: All Default Value: 000b See FP0 CB_Tuning description

Value	Name	Description	Project
000b	Off	CB Tune Off	All
011b	100%	CB Tune 100% On	All

21:16	**FP1_N_Divisor** Project: All Format: N-Divisor value calculated for the desired output frequency. The register value is programmed two less than the actual divisor.
15:14	**Reserved** Project: All Format: MBZ
13:8	**FP1_M1_Divisor** Project: All Format: M-Divisor value calculated for the desired output frequency. The register value is programmed to two less than the actual divisor.
7:6	**Reserved** Project: All Format: MBZ

DPLL_FP1	
5:0	**FP1_M2_Divisor** Project: All Format: M-Divisor value calculated for the desired output frequency. The register value is programmed two less than the actual divisor.

2.3.4 DREF_CONTROL — Display Reference Clock Control Register

DREF_CONTROL — Display Reference Clock Control Register

Register Type: MMIO
Address Offset: C6200h
Project: All
Default Value: 00000000h
Access: R/W
Size (in bits): 32

Bit	Description
31:15	**Reserved** Project: All Format: MBZ
14:13	**120MHz_CPU_source_output_enable** Project: All Default Value: 00b

Value	Name	Description	Project
00b	Disabled	Source output to CPU disabled	All
01b	Reserved	Rerserved	All
10b	Downspread	-0.5% SSC downspread source output to CPU enabled. Both the 120MHz SSC source (bits 12:11) and the SSC1 modulator (bit1) must be enabled prior to enabling this output	All
11b	Non-spread	Non-spread source output to CPU enabled. The 120MHz non-SSC source (bit 10:9) must be enabled prior to enabling this output	All

DREF_CONTROL — Display Reference Clock Control Register

12:11

120MHz_SSC_source_en

Project: All

Default Value: 00b

This bit enables the 120MHz SSC source used as a reference for DisplayPort or CPU

Value	Name	Description	Project
00b	Disabled	Source disabled	All
01b	Reserved	Reserved for CK505 buffered source enabled	All
10b	Enabled	Integrated source enabled	All
11b	Reserved	Reserved	All

10:9

120MHz_nonspread_source_en

Project: All

Default Value: 00b

This field enables the 120MHz non-SSC source for display

Value	Name	Description	Project
00b	Disabled	Source disabled	All
01b	CK505	CK505 buffered source enabled.	All
10b	Integrated	Integrated source enabled	All
11b	Reserved	Reserved	All

8:7

120MHz_superspread_source_en

Project: All

Default Value: 00b

This field enables the 120MHz super-SSC source for display

Value	Name	Description	Project
00b	Disabled	Source disabled	All
01b	Reserved	Reserved	All
10b	Enabled	Integrated source enabled	All
11b	Reserved	Reserved	All

DREF_CONTROL — Display Reference Clock Control Register

6 **SSC4_Spread_Mode**

Project: All

Default Value: 0b

This is the reference clock used for super-spread on LVDS. Please note that this reference is shared with SATA. If it is used for SATA it must not be used for LVDs. This bit must not be changed after bit 0 is set. It may be updated simultaneously with the update of bit 0.

Value	Name	Description	Project
0b	Downspread	Center vs downspread: this bit sets down spread on the SSC4 modulator used for superspread.	All
1b	Centerspread	Center vs downspread: this bit sets center spread on the SSC4 modulator used for superspread.	All

5:2 **Reserved** Project: All Format: MBZ

1 **120MHz_SSC1(-0.5%)modulation_en**

Project: All

Default Value: 0b

This bit enables the -0.5% modulator used for the 120MHz SSC source used for the CPU DisplayPort or as the -0.5% input to the DPLL in the PCH. It must be set 0uS or more after the 120MHz SSC output is enabled (this bit and bits 12:11 can be written to enable at the same time). PLL's using this clock as an input must be enabled 1uS or more after this bit is enabled to ensure a stable input.

Value	Name	Description	Project
0b	Disabled	SSC1 disabled	All
1b	Enabled	SSC1 enabled	All

0 **120MHz_SSC4_modulation_en**

Project: All

Default Value: 0b

This bit enables the variable % modulator used for the 120MHz SSC source used for LVDS. It must be set 0uS or more after the 120MHz super-spread source is enabled (this bit and bits 8:7 can be written to enable at the same time). PLL's using this clock as an input must be enabled 1uS or more after this bit is enabled to ensure a stable input.

Value	Name	Description	Project
0b	Disabled	SSC4 disabled	All
1b	Enabled	SSC4 enabled	All

2.3.5 RAWCLK_FREQ—Rawclk Frequency

RAWCLK_FREQ—Rawclk Frequency	
Register Type:	MMIO
Address Offset:	C6204h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

Bit	Description
31:10	**Reserved** Project: All Format:
9:0	**Rawclk_frequency** Project: All Format: Program this field to match the rawclk frequency. This is used to generate a divided down clock for miscellaneous timers in display. [DevCPT] rawclk = 125mhz

2.3.6 SSC4PARMS – SSC4 Parameters

SSC4PARMS – SSC4 Parameters	
Register Type:	MMIO
Address Offset:	C6210h
Project:	All
Default Value:	01204860h
Access:	R/W
Size (in bits):	32

Notes:

- This register must not be changed after bit 0 of register C6200h is set.
- Default values of this register are meaningless.
- 0% spread option for SSC4 should be configured by clearing bit 0 of C6200h to disable SSC4 module. In this case, registers SSC4PARMS and SSC4AuxPARMS settings have no effect and are don't care to the hardware. Bits 8:7 of C6200h still need to be configured to enable the divisor DIV4, i.e. the source of the clock.
- This register needs to be configured by the display driver for desired spread percentages. Recommended settings for 0.5% down spread and 0.5%, 1.0%, 1.5%, 2.0%, and 2.5% center spread are listed in the following look-up table. Recommended settings for half-step clock bending usage is also listed.

Register fields	half-step clock bend	0.5% down spread	0.5% center spread	1.0% center spread	1.5% center spread	2.0% center spread	2.5% center spread
6/5/4Ni_1NjRpt, [29:28]	00b	01b	01b	01b	01b	01b	01b
3Ni_1NjRpt, [26:24]	000b	010b	010b	010b	010b	010b	010b
2Ni1NjRpt,	000b	111b	111b	111b	111b	111b	111b

SSC4PARMS – SSC4 Parameters

[22:20]							
1Ni1NjRpt, [18:10]	0_0000_0000b	0_0010_1001b	0_0010_1001b	0_0000_0010b	0_0000_1010b	0_0000_0010b	0_0000_1010b
MxPhsStp, [9:3]	000_0000b	000_0101b	000_0010b	000_0101b	000_0100b	000_0101b	000_0100b
PhsIncVal, [2:0]	000b	000b	000b	000b	001b	001b	010b

Bit	Description
31:30	**Reserved** Project: All Format: MBZ
29:28	**SSC4 6/5/4Ni_1Nj Repeat Count (SSC4_6/5/4Ni_1NjRpt)** Project: All Format: U2+1 Default Value: 00b 1 times Select the number of repeats for the portion of 4, or 5, or 6 clocks of Ni and 1 clock of Nj within a dithering pattern of a step. See 1Ni_1Nj Repeat Count for more information.
27	**Reserved** Project: All Format: MBZ
26:24	**SSC4 3Ni_1Nj Repeat Count (SSC4_3Ni_1NjRpt)** Project: All Format: U3+1 Default Value: 001b 2 times Select the number of repeats for the portion of 3 clocks of Ni and 1 clock of Nj within a dithering pattern of a step. See 1Ni_1Nj Repeat Count for more information.
23	**Reserved** Project: All Format: MBZ
22:20	**SSC4 2Ni_1Nj Repeat Count (SSC4_2Ni1NjRpt)** Project: All Format: U3+1 Default Value: 010b 3 times Select the number of repeats for the portion of 2 clocks of Ni and 1 clock of Nj within a dithering pattern of a step. See 1Ni_1Nj Repeat Count for more information.
19	**Reserved** Project: All Format: MBZ
18:10	**SSC4 1Ni_1Nj Repeat Count (SSC4_1Ni1NjRpt)** Project: All Format: U9+1 Default Value: 000010010b 19 times Select the number of repeats for the portion of 1 clock of Ni and 1 clock of Nj within a dithering pattern of a step. Together, 1Ni_1Nj Repeat Count, 2Ni_1Nj Repeat Count, 3Ni_1Nj Repeat Count, and 6/5/4Ni_1Nj Repeat Count tune the width of the target 32Khz modulated period. For down spread, the target these fields are to be tuned to is one half of the modulated period. For center spread, the target is one quarter of the modulated period.
9:3	**SSC4 Max Phase Step (SSC4_MxPhsStp)** Project: All Format: U7+1 Default Value: 0001100b 13 steps Select the number of steps to reach peak of modulated phase adjustment value. Together, Max Phase Step field and Phase Increment Value field control the magnitude of the spread.

SSC4PARMS – SSC4 Parameters	
2:0	**SSC4 Phase Increment Value (SSC4_PhsIncVal)** Project: All Format: U3+1 Default Value: 000b 1 PI change per step Select the granularity of each phase step. Together, Max Phase Step field and Phase Increment Value field control the magnitude of the spread.

2.3.7 DPLL_SEL— DPLL Select

DPLL_SEL

Register Type: MMIO
Project: All
Default Value: 00000000h
Access: R/W
Size (in bits): 32

Individual bits are write protected by panel power sequencing when the panel is connected to the transcoder associated with that bit.

Bit	Description
31:12	**Reserved** Project: All Format:
11	**Transcoder_C_DPLL_Enable** Project: All Default Value: 0b

Value	Name	Description	Project
0b	Disable	Disable DPLL to this transcoder	All
1b	Enable	Enable DPLL to this transcoder	All

10:9	**Reserved** Project: All Format:
8	**Transcoder_C_DPLL_Select** Project: All Default Value: 0b

Value	Name	Description	Project
0b	DPLLA	Select DPLLA for this transcoder	All
1b	DPLLB	Select DPLLB for this transcoder	All

DPLL_SEL

7 — **Transcoder_B_DPLL_Enable**

Project: All

Default Value: 0b

Value	Name	Description	Project
0b	Disable	Disable DPLL to this transcoder	All
1b	Enable	Enable DPLL to this transcoder	All

6:5 — **Reserved** Project: All Format:

4 — **Transcoder_B_DPLL_Select**

Project: All

Default Value: 0b

Value	Name	Description	Project
0b	DPLLA	Select DPLLA for this transcoder	All
1b	DPLLB	Select DPLLB for this transcoder	All

3 — **Transcoder_A_DPLL_Enable**

Project: All

Default Value: 0b

Value	Name	Description	Project
0b	Disable	Disable DPLL to this transcoder	All
1b	Enable	Enable DPLL to this transcoder	All

2:1 — **Reserved** Project: All Format:

0 — **Transcoder_A_DPLL_Select**

Project: All

Default Value: 0b

Value	Name	Description	Project
0b	DPLLA	Select DPLLA for this transcoder	All
1b	DPLLB	Select DPLLB for this transcoder	All

2.4 Panel Power Sequencing Registers

2.4.1 PP_STATUS—Panel Power Status Register

PP_STATUS

Register Type: MMIO
Project: All
Default Value: 08000000h
Access: Read Only
Size (in bits): 32

Bit	Description
31	**Panel_Power_On_Status** Project: All Default Value: 0b Software is responsible for enabling the embedded panel display by writing a "1" to the port enable bit only after all pipe and transcoder timing and DPLL registers are properly programmed and the PLL has locked to the reference signal. This bit is cleared to "0" only after the panel power down sequencing is completed.

Value	Name	Description	Project
0b	Off	Indicates that the panel power down sequencing has completed. A power cycle delay may be currently active. It is safe and allowed to program timing, port, and DPLL registers. If this bit is not a zero, it activates the register write protect and writes to those registers will be ignored unless the write protect key value is set in the panel sequencing control register.	All
1b	On	In conjunction with bits Power Sequence Progress field and Power Cycle Delay Active, this bit set to a one indicates that the panel is currently powered up or is currently in the power down sequence and it is unsafe to change the timing, port, and DPLL registers for the pipe or transcoder that is assigned to the panel output.	All

Bit	Description
30	**Require_Asset_Status** Project: All Default Value: 0b This bit indicates the status of programming of the DPLL and the selected port. A power on cycle will not be allowed unless this status indicates that the required assets are programmed and ready for use. The following conditions determine that the assets are ready: 1) Display pipe or transcoder PLL enabled and frequency locked. 2) Display pipe or transcoder enabled. 3) Port attached to the panel is enabled.

Value	Name	Description	Project
0b	Not Ready	All required assets are not properly programmed	All
1b	Ready	All required assets are ready for the driving of a panel	All

PP_STATUS

29:28 Power_Sequence_Progress

Project: All

Default Value: 0b

Value	Name	Description	Project
00b	None	Indicates that the panel is not in a power sequence	All
01b	Power Up	Indicates that the panel is in a power up sequence (may include power cycle delay)	All
10b	Power Down	Indicates that the panel is in a power down sequence	All
11b	Reserved	Reserved	All

27 Power_Cycle_Delay_Active

Project: All

Default Value: 1b A power cycle delay (T4) is currently active

Power cycle delays occur after a panel power down sequence or after a hardware reset. On reset, a power cycle delay will occur using the default value for the timing.

Value	Name	Description	Project
0b	Not Active	A power cycle delay is not currently active	All
1b	Active	A power cycle delay (T4) is currently active	All

26:4 Reserved Project: All Format:

3:0 Reserved

Project: All

2.4.2 PP_CONTROL—Panel Power Control Register

PP_CONTROL—Panel Power Control Register	
Register Type:	MMIO
Address Offset:	C7204h
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

Bit	Description
31:16	**Write_Protect_Key** Project: All Default Value: 0b This field can be programmed with the key value "ABCD" to uncoditionally disable write protect. This field must be programmed with the value 0xABCD when using panel power sequencing on DisplayPort A (PP_ON_DELAYS bits 31:30 Panel_Control_port_select is set to 01b for DisplayPort A).
15:4	**Reserved** Project: All Format:
3	**eDP_VDD_Override_for_AUX** Project: All Default Value: 0b This bit is used to force on VDD for the embedded DP panel so AUX transactions can occur without enabling the panel power sequence. This is intended for panels that require VDD to be asserted before accessing AUX port on the receiver. When software clears this bit from '1' to '0' (disable VDD override) it must ensure that T4 power cycle delay is met before setting this bit to '1' again.

Value	Name	Description	Project
0b	Not Force	VDD controlled by Panel Power Sequence state machine	All
1b	Force	Force VDD on to allow AUX transaction. Panel power sequence flow should be used regardless of the state of this bit when it is desired to enable the embedded DP main link.	All

PP_CONTROL—Panel Power Control Register

2

Backlight_Enable

Project: All

Default Value: 0b

Enabling this bit enables the panel backlight if the embedded panel is DisplayPort, as indicated in bits 31:30 of the panel power on sequencing. Software must enable this bit after training the link, and disable it when disabling the panel power state target.

Value	Name	Description	Project
0b	Disable	Backlight disabled	All
1b	Enable	Backlight enabled	All

1

Power_Down_on_Reset

Project: All

Default Value: 0b

Enabling this bit causes the panel to power down on reset warning. When system reset is initiated, the panel power down sequence begins automatically. If the panel is not on during a reset event, this bit is ignored.

This bit must be cleared to 0b prior to initiating a panel power up or power down sequence, then this bit must be restored after the sequence completes.

Value	Name	Description	Project
0b	Do not Run	Do not run panel power down sequence when reset is detected	All
1b	Run	Run panel power down sequence when system is reset	All

0

Power_State_Target

Project: All

Default Value: 0b

Writing this bit can occur any time, it will only be used at the completion of any current power cycle.

Value	Name	Description	Project
0b	Off	The panel power state target is off, if the panel is either on or in a power on sequence, a power off sequence is started as soon as the panel reaches the power on state. This may include a power cycle delay. If the panel is currently off, there is no change of the power state or sequencing done.	All
1b	On	The panel power state target is on, if the panel is in either the off state or a power off sequence, if all pre-conditions are met, a power on sequence is started as soon as the panel reaches the power off state. This may include a power cycle delay. If the panel is currently off, there is no change of the power state or sequencing done. While the panel is on or in a power on sequence, the register write lock will be enabled.	All

2.4.3 PP_ON_DELAYS—Panel Power On Sequencing Delays

PP_ON_DELAYS—Panel Power On Sequencing Delays

Register Type: MMIO
Address Offset: C7208h
Project: All
Default Value: 00000000h
Access: R/W Protect
Size (in bits): 32

Write Protect by Panel Power Sequencer

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>31:30</td><td>Panel_Control_port_select
Project: All
Default Value: 0b
These bits define to which port the embedded panel is connected. This is used for automatic control of the panel power. If the selected port is disabled then, the power sequence will not allow a panel power up.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr>
<tr><td>00b</td><td>LVDS</td><td>Panel is connected to the LVDS display port</td><td>All</td></tr>
<tr><td>01b</td><td>DPA</td><td>Panel is connected to the DisplayPort A
PP_CONTROL 0xC7204 bits 31:16 Write_Protect_Key must be programmed to 0xABCD when using panel power sequencing on DisplayPort A.</td><td>All</td></tr>
<tr><td>10b</td><td>DPC</td><td>Panel is connected to the DisplayPort C</td><td>All</td></tr>
<tr><td>11b</td><td>DPD</td><td>Panel is connected to the DisplayPort D</td><td>All</td></tr>
</table></td></tr>
<tr><td>29</td><td>Reserved Project: All Format:</td></tr>
<tr><td>28:16</td><td>Power_up_delay Project: All Format:
Programmable value of panel power sequencing delay during panel power up. This provides the time delay for the T1+T2 time sequence. The time unit used is the 100us timer.</td></tr>
<tr><td>15:13</td><td>Reserved Project: All Format:</td></tr>
<tr><td>12:0</td><td>Power_on_to_Backlight_enable_delay Project: All Format:
Programmable value of panel power sequencing delay during panel power up. This provides the time delay for the T5 time sequence. The time unit used is the 100us timer.</td></tr>
</table>

2.4.4 PP_OFF_DELAYS—Panel Power Off Sequencing Delays

PP_OFF_DELAYS—Panel Power Off Sequencing Delays	
Register Type:	MMIO
Address Offset:	C720Ch
Project:	All
Default Value:	00000000h
Access:	R/W Protect
Size (in bits):	32
Write Protect by Panel Power Sequencer	

Bit	Description
31:29	**Reserved** Project: All Format:
28:16	**Power_Down_delay** Project: All Format: Programmable value of panel power sequencing delay during power up. This provides the time delay for the T3 time sequence. The time unit used is the 100us timer.
15:13	**Reserved** Project: All Format:
12:0	**Backlight_off_to_power_down** Project: All Format: Power backlight off to power down delay. Programmable value of panel power sequencing delay during power down. This provides the time delay for the Tx time sequence. The time unit used is the 100us timer.

2.4.5 PP_DIVISOR—Panel Power Cycle Delay and Reference Divisor

PP_DIVISOR—Panel Power Cycle Delay and Reference Divisor

Register Type: MMIO
Address Offset: C7210h
Project: All
Default Value: 00186904h
Access: R/W Protect
Size (in bits): 32

Write Protect by Panel Power Sequencer

This register selects the reference divisor and controls how long the panel must remain in a power off condition once powered down. This has a default value that allows a timer to initiate directly after device reset. If the panel limits how fast we may sequence from up to down to up again. Typically this is 0.5-1.5 seconds, but limited to 400ms in the SPWG specification. This register forces the panel to stay off for a programmed duration. Special care is needed around reset and D3 cold situations to conform to power cycle delay specifications.

Bit	Description
31:8	**Reference_divider** Project: All Default Value: 001869h 125MHz raw clock. This field provides the value of the divider used for the creation of the panel timer reference clock. The output of the divider is used as the fastest of the three time bases (100us) for all other timers. The other time bases are divided from this frequency. The value of zero should not be used. When it is desired to divide by N, the actual value to be programmed is (N/2)-1. The value should be (100 * Ref clock frequency in MHz / 2) - 1. The default value is for the 125MHz raw clock. **Example:** **Reference Clock Frequency** **Value of Field** 233MHz 2D81h 200MHz 270Fh 125MHz 1869h
7:5	**Reserved** Project: All Format:
4:0	**Power_Cycle_Delay** Project: All Format: Programmable value of time panel must remain in a powered down state after powering down. For devices coming out of reset, the default values will define how much time must pass before a power on sequence can be started. This field uses the 0.1 S time base unit from the divider. If the panel power on sequence is attempted during this delay, the power on sequence will commence once the power cycle delay is complete. Writing a value of 0 selects no delay or is used to abort the delay if it is active. During the initial power up reset, a D3 cold power cycle, or a user instigated system reset, the timer will be set to the default value and the count down will begin after the de-assertion of reset. Writing this field to a zero while the count is active will abort this portion of the sequence. This corresponds to the T4 of the SPWG specification. Note: Even if the panel is not enabled, the T4 count happens after reset. This register needs to be programmed to a “+1” value. For instance for meeting the SPWG specification of 400mS, program 5 to achieve at least 400mS delay prior to powerup.

2.5 Backlight Control Registers

2.5.1 Backlight PWM PCH Control Register 1

Backlight PWM PCH Control Register 1

Register Type: MMIO
Address Offset: C8250h
Project: All
Default Value: 00000000h
Access: R/W
Size (in bits): 32

Bit	Description
31	**PWM_PCH_Enable** Project: All Default Value: 0b This bit enables the PWM counter logic in the PCH.

Value	Name	Description	Project
0b	Disable	PCH PWM disabled (drives 0 always)	All
1b	Enable	PCH PWM enabled	All

Bit	Description
30	**PWM_PCH_Override_Enable** Project: All Default Value: 0b This bit enables PWM messages from CPU to PCH to be overriden by the Backlight PWM PCH Control Register Backlight Duty Cycle Override value.

Value	Name	Description	Project
0b	Disable	Override disabled (CPU messages control PWM duty cycle)	All
1b	Enable	Override enabled (Override register value controls PWM duty cycle)	All

Bit	Description
29	**Backlight_Polarity** Project: All Default Value: 0b This field controls the polarity of the PWM signal.

Value	Name	Description	Project
0b	High	Active High	All
1b	Low	Active Low	All

Bit	Description
28	**Reserved** Project: All Format:
27:0	**Reserved** Project: All Format:

2.5.2 SBLC_BLM_CTL2—South BLM Control 2

SBLC_PWM_CTL2	
Register Type:	MMIO
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

Bit	Description
31:16	**Backlight_Modulation_Frequency** Project: All Format: This field determines the number of time base events in total for a complete cycle of modulated backlight control. This field is normally set once during initialization based on the frequency of the clock that is being used and the desired PWM frequency. This value represents the period of the PWM stream in PCH display raw clocks multiplied by 128.
15:0	**Backlight_Duty_Cycle_Override** Project: All This value overrides the CPU control of PWM duty cycle when the PWM PCH Override Enable bit is set. This field determines the number of time base events for the active portion of the PWM backlight control. This should never be larger than the frequency field. A value of zero will turn the backlight off. A value equal to the backlight modulation frequency field will be full on. This field gets updated when it is desired to change the intensity of the backlight, it will take affect at the end of the current PWM cycle. This value represents the active time of the PWM stream in PCH display raw clock periods multiplied by 128.

3. South Display Engine Transcoder and Port Controls

3.1 Transcoder Timing

3.1.1 HTOTAL—Horizontal Total

HTOTAL	
Register Type: MMIO **Project:** All **Default Value:** 00000000h **Access:** R/W **Size (in bits):** 32 Write Protect by Panel Power Sequencer when panel is connected to this transcoder.	
Bit	**Description**
31:29	**Reserved** Project: All Format: MBZ
28:16	**Horizontal_Total** Project: All This field specifies Horizontal Total size. This should be equal to the sum of the horizontal active and the horizontal blank sizes. This field is programmed to the number of pixels desired minus one. The number of pixels (before the minus one) needs to be a multiple of two when driving the LVDS port in two channel mode. This register must always be programmed to the same value as the Horizontal Blank End.
15:12	**Reserved** Project: All Format: MBZ
11:0	**Horizontal_Active** Project: All This field specifies Horizontal Active Display size. Note that the first horizontal active display pixel is considered pixel number 0. This field is programmed to the number of pixels desired minus one. The number of pixels (before the minus one) needs to be a multiple of two when driving the LVDS port in two channel mode. The minimum horizontal active display size is 64 pixels. This register must always be programmed to the same value as the Horizontal Blank Start.

3.1.2 HBLANK—Horizontal Blank

HBLANK	
Register Type: MMIO **Project:** All **Default Value:** 00000000h **Access:** R/W **Size (in bits):** 32 Write Protect by Panel Power Sequencer when panel is connected to this transcoder.	
Bit	**Description**
31:29	**Reserved** Project: All Format:
28:16	**Horizontal_Blank_End** Project: All This field specifies Horizontal Blank End position relative to the horizontal active display start. The number of pixels within horizontal blank needs to be a multiple of two when driving the LVDS port in two channel mode. The minimum horizontal blank size is 32 pixels. This register must always be programmed to the same value as the Horizontal Total.
15:13	**Reserved** Project: All Format:
12:0	**Horizontal_Blank_Start** Project: All This field specifies the Horizontal Blank Start position relative to the horizontal active display start. This register must always be programmed to the same value as the Horizontal Active.

3.1.3 HSYNC—Horizontal Sync

HSYNC	
Register Type: MMIO **Project:** All **Default Value:** 00000000h **Access:** R/W **Size (in bits):** 32 Write Protect by Panel Power Sequencer when panel is connected to this transcoder.	
Bit	**Description**
31:29	**Reserved** Project: All Format: MBZ
28:16	**Horizontal_Sync_End** Project: All Default Value: 0b This field specifies the Horizontal Sync End position relative to the horizontal active display start. It is programmed with HorizontalActive+FrontPorch+Sync-1 HDMI and DVI with audio are not supported when HSYNC Start is programmed equal to HBLANK Start. The number of pixels within horizontal sync needs to be a multiple of two when driving the LVDS port in two channel mode. This value must be greater than the horizontal sync start and less than Horizontal Total.
15:13	**Reserved** Project: All Format: MBZ
12:0	**Horizontal_Sync_Start** Project: All Default Value: 0b This field specifies the Horizontal Sync Start position relative to the horizontal active display start. It is programmed with HorizontalActive+FrontPorch-1 The number of pixels from active to horizontal sync needs to be a multiple of two when driving the LVDS port in two channel mode This value must be greater than Horizontal Active.

3.1.4 VTOTAL—Vertical Total

VTOTAL	
Register Type: MMIO **Project:** All **Default Value:** 00000000h **Access:** R/W **Size (in bits):** 32 Write Protect by Panel Power Sequencer when panel is connected to this transcoder.	
Bit	**Description**
31:29	**Reserved** Project: All Format:
28:16	**Vertical_Total** Project: All This field specifies Vertical Total size. This should be equal to the sum of the vertical active and the vertical blank sizes. For progressive display modes, this field is programmed to the number of lines desired minus one. For interlaced display modes, this field is programmed with the number of lines desired minus two. The vertical counter is incremented on the leading edge of the horizontal sync. For interlaced display, hardware uses this value to calculate the vertical total in each field. Note that both even and off vertical totals are supported. This register must always be programmed to the same value as the Vertical Blank End.
15:12	**Reserved** Project: All Format:
11:0	**Vertical_Active** Project: All This field specifies Vertical Active Display size. Note that the first vertical active display line is considered pixel number 0. This field is programmed to the number of lines desired minus one. When using the internal panel fitting logic, the minimum vertical active area must be seven lines. For interlaced display, hardware uses this value to calculate the vertical active in each field. This register must always be programmed to the same value as the Vertical Blank Start.

3.1.5 VBLANK—Vertical Blank

VBLANK	
Register Type: MMIO **Project:** All **Default Value:** 00000000h **Access:** R/W **Size (in bits):** 32 Write Protect by Panel Power Sequencer when panel is connected to this transcoder.	
Bit	**Description**
31:29	**Reserved** Project: All Format:
28:16	**Vertical_Blank_End** Project: All This field specifies Vertical Blank End position relative to the vertical active display start. The minimum vertical blank size is 5 lines. For interlaced display, hardware uses this value to calculate the vertical blank end in each field. This register must always be programmed to the same value as the Vertical Total.
15:13	**Reserved** Project: All Format:
12:0	**Vertical_Blank_Start** Project: All This field specifies the Vertical Blank Start position relative to the vertical active display start. For interlaced display, hardware uses this value to calculate the vertical blank start in each field. This register must always be programmed to the same value as the Vertical Active

3.1.6 VSYNC—Vertical Sync

VSYNC	
Register Type: MMIO **Project:** All **Default Value:** 00000000h **Access:** R/W **Size (in bits):** 32 Write Protect by Panel Power Sequencer when panel is connected to this transcoder.	
Bit	**Description**
31:29	**Reserved** Project: All Format:
28:16	**Vertical_Sync_End** Project: All This field specifies the Vertical Sync End position relative to the vertical active display start. It is programmed with VerticalActive+FrontPorch+Sync-1 For interlaced display, hardware uses this value to calculate the vertical sync start in each field. This value must be greater than the vertical sync start and less than Vertical Total.
15:13	**Reserved** Project: All Format:
12:0	**Vertical_Sync_Start** Project: All This field specifies the Vertical Sync Start position relative to the vertical active display start. It is programmed with VerticalActive+FrontPorch-1 For interlaced display, hardware uses this value to calculate the vertical sync end in each field. This value must be greater than Vertical Active.

3.1.7 VSYNCSHIFT— Vertical Sync Shift

VSYNCSHIFT	
Register Type: MMIO **Project:** All **Default Value:** 00000000h **Access:** R/W **Size (in bits):** 32 Write Protect by Panel Power Sequencer when panel is connected to this transcoder.	
Bit	**Description**
31:13	**Reserved** Project: All Format:
12:0	**Second_Field_VSync_Shift** Project: All This value specifies the vertical sync alignment for the start of the interlaced second field, expressed in terms of the absolute pixel number relative to the horizontal active display start. This value will only be used if the transcoder is in an interlaced mode. Typically, the interlaced second field vertical sync should start one pixel after the point halfway between successive horizontal syncs, so the value of this register should be programmed to: horizontal sync start - floor[horizontal total / 2] (use the actual horizontal sync start and horizontal total values and not the minus one values programmed into the registers) Legacy operation can be simulated by programming a value of floor[htotal / 2] (use the programmed minus one horizontal total value). This vertical sync shift only occurs during the interlaced second field. In all other cases the vertical sync start position is aligned with horizontal sync start.

3.2 Transcoder M/N Values

These values are used for DisplayPort.

When switching between two refresh rates, both the M1/N1 data and link values and the M2/N2 link values must be programmed. For dynamic refresh rate control, M1/N1 values are the primary values and are used for the normal M/N value setting, and M2/N2 values are the secondary values and are used for the lower power M/N value setting. Selection of M1/N1 or M2/N2 is indicated via MSA from the CPU display.

Example calculation of TU, Data M, and Data N: (See DisplayPort specification for exact calculation)

For modes that divide into the link frequency evenly,

Active/TU = Payload/Capacity = Data M/N = dot clock * bytes per pixel / ls_clk * number of lanes

Default value to program TU size is "111111" for TU size of 64.

Calculation of Link M and Link N:

Link M/N = dot clock / ls_clk

Restriction on clocks and number of lanes:
Number of lanes >= INT(dot clock * bytes per pixel / ls_clk)
Pcdclk * number of lanes >= dot clock * bytes per pixel

Please note that in the DisplayPort specification, dot clock is referred to as strm_clk.

3.2.1 DATAM— Data M Value

DATAM	
Register Type:	MMIO
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank
Double Buffer Armed By:	Writing the LINKN

Bit	Description
31	**Reserved** Project: All Format: MBZ
30:25	**TU_Size** Project: All This field is the size of the transfer unit, minus one.
24	**Reserved** Project: All Format: MBZ
23:0	**Data_M_value** Project: All This field is the m value for internal use of the DDA.

3.2.2 DATAN— Data N Value

DATAN	
Register Type:	MMIO
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank
Double Buffer Armed By:	Writing the LINKN

Bit	Description
31:24	**Reserved** Project: All Format: MBZ
23:0	**Data_N_value** Project: All This field is the n value for internal use of the DDA.

3.2.3 LINKM— Link M Value

LINKM	
Register Type:	MMIO
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank
Double Buffer Armed By:	Writing the LINKN

Bit	Description
31:24	**Reserved** Project: All Format: MBZ
23:0	**Link_M_value** Project: All This field is the m value for external transmission in the Main Stream Attributes.

3.2.4 LINKN— Link N Value

LINKN	
Register Type:	MMIO
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank

Writes to this register arm M/N registers for this transcoder.

Bit	Description
31:24	**Reserved** Project: All Format: MBZ
23:0	**Link_N_value** Project: All This field is the n value for external transmission in the Main Stream Attributes and VB-ID.

3.3 Transcoder Video DIP

3.3.1 VIDEO_DIP_CTL—Video DIP Control

VIDEO_DIP_CTL	
Register Type:	MMIO
Project:	All
Default Value:	20000900h
Access:	R/W
Size (in bits):	32

Please note that writes to this register take effect immediately. Therefore, it is critical for software to follow the write and read sequences as described in the bit 31 text.

Bit	Description
31	**Enable_Graphics_DIP** Project: All Default Value: 0b Data Island Packet (DIP) is a mechanism that allows up to 36 bytes to be sent over digital port during VBLANK, according to the HDMI and DisplayPort specifications. This includes header, payload, checksum and ECC information. Each type of DIP can be sent once per vsync, once every other vsync, or once. This data can be transmitted on either transcoder, through any digital port (digital port B, C or D), but not two simultaneously on one transcoder. Please note that the audio subsystem is also capable of sending Data Island Packets. These packets are programmed by the audio driver and can be read by in MMIO space via the audio control state and audio HDMI widget data island registers. Write sequence: 1. Wait for 1 VSync to ensure completion of any pending DIP transmissions. 2. Disable the Video_DIP_type_enable and set the Video_DIP_buffer_index for the DIP being written. 3. Set the Video_DIP_access_address to the desired DWORD to be written. 4. Write DIP data 1 DWORD at a time. The DIP access address auto-increments with each DWORD write, wrapping around to address 0 when the max buffer address size has been reached. Please note that software must write an entire DWORD at a time. 5. Enable the DIP type and transmission frequency. Read sequence: 1. Set the Video_DIP_buffer_index for the DIP being read. 2. Set the Video_DIP_access_address to the desired DWORD to be read. 3. Read DIP data 1 DWORD at a time. The DIP access address auto-increments with each DWORD read, wrapping around to address 0 when the max buffer address size has been reached.

VIDEO_DIP_CTL

Register Type: MMIO
Project: All
Default Value: 20000900h
Access: R/W
Size (in bits): 32

Please note that writes to this register take effect immediately. Therefore, it is critical for software to follow the write and read sequences as described in the bit 31 text.

Bit | **Description**

Value	Name	Description	Project
0b	Disable	Video DIP is disabled	All
1b	Enable	Video DIP is enabled	All

Programming Notes

- Partial DIPs are never sent out while the port is enabled. Disabling the DIP at the same time it is being transferred will result in the DIP being completed before the function is disabled.
- Shutting off the port on which DIP is being transmitted will result in partial transfer of DIP data. There is no need to switch off the DIP enable bit if the port transmitting DIP is disabled.
- When disabling both the DIP port and DIP transmission, first disable the port and then disable DIP.
- Enabling a DIP function at the same time that the DIP would have been sent out (had it already been enabled) will result in the DIP being sent on the following frame.
- Enabling should only be done after the buffer contents have been written.
- If DIP is enabled but DIP types are all disabled, no DIP is sent. However, a single Null DIP will be sent at the same point in the stream that DIP packets would have been sent. This is done to keep the port in HDMI mode, otherwise it would revert to DVI mode. HDMI_CTL Null_packets_enabled_during_vsync overrides this behavior.
- Enable_Graphics_DIP (bit 31) and Data_Island_Packet_type_enable for AVI (bit 23) must be set or cleared in the same write if the HDMI port is already enabled

30:26 **Reserved** Project: All Format:

25 **GCP_DIP_enable**

Project: All

Default Value: 0b

This bit enables the output of the General Control Packet. GCP is different from other DIPs in that much of the payload is automatically reflected in the packet, and therefore a DIP buffer for GCP is not needed. Please refer to the GCP payload register for payload details. Writes to this bit take effect immediately.

Software must enable this bit before enabling the port when GCP is required, and disable this bit after disabling the port.

Value	Name	Description	Project
0b	Disable	GCP DIP disabled	All
1b	Enable	GCP DIP enabled	All

VIDEO_DIP_CTL

Register Type: MMIO
Project: All
Default Value: 20000900h
Access: R/W
Size (in bits): 32

Please note that writes to this register take effect immediately. Therefore, it is critical for software to follow the write and read sequences as described in the bit 31 text.

Bit	Description
24:21	**Video_DIP_type_enable** Project: All Default Value: 0001b Enable AVI DIP These bits enable the output of a given data island packet type. It can be updated while the port is enabled and is immediately updated (not double-buffered). Within 2 vblank periods, the DIP is guaranteed to have been transmitted. Software must enable VS DIP type (initialized to zero or programmed with valid VS payload) in addition when it is desired to enable AVI+SPD+GMP AVI enable (bit 23) and Enable_Graphics_DIP (bit 31) must be set or cleared in the same write if the HDMI port is already enabled. AVU should be updated dynamically (without clearing the enable bit) by waiting for vertical blank and then updating the AVI buffer.

Value	Name	Description	Project
XXX1b	Enable AVI	Enable AVI DIP	All
XX1Xb	Enable Vendor	Enable Vendor-specific DIP	All
X1XXb	Enable Gamut	Enable Gamut Metadata Packet	All
1XXXb	Enable Source	Enable Source Product Description DIP	All

Bit	Description
20:19	**Video_DIP_buffer_index** Project: All Default Value: 00b This field is used during programming of different DIPs. These bits are used as an index to their respective DIP buffers. The transmission frequency must also be written when programming the buffer.

Value	Name	Description	Project
00b	AVI	AVI DIP (31 bytes of space available)	All
01b	Vendor-specific	Vendor-specific DIP	All
10b	Gamut Metadata	Gamut Metadata Packet	All
11b	Source Product	Source Product Description DIP	All

Bit	Description
18	**Reserved** Project: All Format:

VIDEO_DIP_CTL

Register Type: MMIO
Project: All
Default Value: 20000900h
Access: R/W
Size (in bits): 32

Please note that writes to this register take effect immediately. Therefore, it is critical for software to follow the write and read sequences as described in the bit 31 text.

Bit	Description
17:16	**Video_DIP_frequency** Project: All Default Value: 00b These bits dictate the frequency of Video DIP transmission for the DIP buffer index designated in bits 20:19. When writing Video DIP data, this value is also latched when the first DW of the Video DIP is written. When read, this value reflects the Video DIP transmission frequency for the Video DIP buffer designated in bits 20:19. This field shall be ignored for Gamut Metadata Packet transmission. Always program AVI to "Send Every Vsync" when enabling AVI.
15:12	**Reserved** Project: All Format: MBZ
11:8	**Video_DIP_buffer_size** Project: All Access: Read Only Default Value: 1001b This reflects the buffer size in dwords available for the type of Video DIP being indexed by bits 20:19 of this register, including the header. It is hardwired to the maximum size of a Video DIP, 36 bytes. Please note that this count includes ECC bytes, which are not writable by software. These bits are immediately valid after write of the DIP index.
7:4	**Reserved** Project: All Format: MBZ
3:0	**Video_DIP_access_address** Project: All Selects the DWORD address for access to the Video DIP buffers. This value is automatically incremented after each read or write of the Video DIP Data Register. The value wraps back to zero when it autoincrements past the max address value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.

Value	Name	Description	Project
00b	Send Once	Send Once	All
01b	Every VSync	Send Every VSync (Default for AVI)	All
10b	Every Other Vsync	Send at least every other VSync	All
11b	Reserved	Reserved	All

3.3.2 VIDEO_DIP_DATA–Video Data Island Packet Data

VIDEO_DIP_DATA	
Register Type:	MMIO
Project:	All
Default Value:	00000000h
Access:	R/W (DWORD access only, no byte access)
Size (in bits):	32

Bit	Description
31:0	**Video_DIP_DATA** Project: All When read, this returns the current value at the location specified in the Video DIP buffer index select and Video DIP access address fields. The address index is incremented after each read or write of this register. DIP data can be read at any time. Data should be loaded before enabling the transmission through the DIP type enable bit.

Construction of DIP Data:

Dword	Byte3	Byte2	Byte1	Byte0
0	DP : HB3 HDMI: ECC (RO)	HB2	HB1	HB0
1	DB3	DB2	DB1	DB0
2	DB7	DB6	DB5	DB4
3	DB11	DB10	DB9	DB8
4	DB15	DB14	DB13	D12
5	DB19	DB18	DB17	DB16
6	DB23	DB22	DB21	DB20
7	DB27	DB26	DB25	DB24
8	ECC byte3 (RO)	ECC byte2 (RO)	ECC byte1 (RO)	ECC byte0 (RO)
9	DP: ECC byte7 (RO) HDMI : Reserved	DP: ECC byte6 (RO) HDMI : Reserved	DP: ECC byte5 (RO) HDMI : Reserved	DP: ECC byte4 (RO) HDMI : Reserved
10	DP: ECC byte11 (RO) HDMI : Reserved	DP: ECC byte10 (RO) HDMI : Reserved	DP: ECC byte9 (RO) HDMI : Reserved	DP: ECC byte8 (RO) HDMI : Reserved
11	Reserved	Reserved	Reserved	Reserved
12	Reserved	Reserved	Reserved	Reserved

Dword	Byte3	Byte2	Byte1	Byte0
13	Reserved	Reserved	Reserved	Reserved
14	Reserved	Reserved	Reserved	Reserved
15	Reserved	Reserved	Reserved	Reserved

HB = Header Byte

DB = Data Byte

DP = DisplayPort

3.3.3 VIDEO_DIP_GCP–Video Data Island Payload

VIDEO_DIP_GCP

Register Type: MMIO
Project: All
Default Value: 00000000h
Access: R/W
Size (in bits): 32

Bit	Description
31:3	**Reserved** Project: All Format: MBZ
2	**GCP_color_indication** Project: All Default Value: 0b This bit must be set when in deep color mode. It may optionally be set for 24-bit mode. It must be set if the sink attached to the transcoder can receive GCP data.

Value	Name	Description	Project
0b	Don't Indicate	Don't indicate color depth. CD and PP bits in GCP set to zero	All
1b	Indicate	Indicate color depth using CD bits in GCP. It will be set depending on programmed pixel depth in port control register	All

VIDEO_DIP_GCP

1

GCP_default_phase_enable

Project: All

Default Value: 0b

Indicates the video timings meet alignment requirements such that the following conditions are met:

1) Htotal is an even number

2) Hactive is an even number

3) Hsync is an even number

4) Front and back porches for Hsync are even numbers

5) Vsync always starts on an even-numbered pixel within a line in interlaced modes (starting counting with 0)

Value	Name	Description	Project
0b	Clear	Default phase bit in GCP is cleared	All
1b	Require Met	Default phase bit in GCP is set. All requirements must be met before setting this bit	All

0

GCP_AV_mute

Project: All

Default Value: 0b

Set AV mute bit in GCP.

Value	Name	Description	Project
0b	Clear	AV mute bit in GCP is cleared. When this bit transitions to 0, the AV mute clear flag is sent in the next GCP packet	All
1b	Set	AV mute bit in GCP is set. When this bit transitions to 1, the AV mute set flag is sent in the next GCP packet	All

3.4 Transcoder DisplayPort Control

3.4.1 TRANS_DP_CTL—Transcoder DisplayPort Control

TRANS_DP_CTL	
Register Type:	MMIO
Project:	All
Default Value:	60000018h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Depends on bit

This register configures transcoder based DisplayPort logic. This register must be used in conjunction with the DisplayPort Control registers.

Bit	Description
31	**Transcoder_DP_Output_Enable** Project: All Default Value: 0b This bit determines if this transcoder will output to a DisplayPort. Transcoder_DP_Port_Select needs to be set to 11b (None) when writing a 0b to this bit to disable transcoder output to DisplayPort.
30:29	**Transcoder_DP_Port_Select** Project: All Default Value: 11b Reserved This bit determines which DisplayPort port block will be driven by the DisplayPort output of this transcoder. Port selection takes place on the Vblank after being written. This field needs to be set to 11b (None) when writing a 0b to Transcoder_DP_Output_Enable to disable transcoder output to DisplayPort.
28:27	**Reserved** Project: All Format: MBZ
26:19	**Reserved** Project: All Format: MBZ

Value	Name	Description	Project
0b	Disable	Disable the transcoder output to DisplayPort	All
1b	Enable	Enable the transcoder to output to DisplayPort	All

Value	Name	Description	Project
00b	Port B	DisplayPort Port B	All
01b	Port C	DisplayPort Port C	All
10b	Port D	DisplayPort Port D	All
11b	None	No port selected	All

TRANS_DP_CTL

18	**Transcoder_DP_Enh_Framing** Project: All Default Value: 0b This bit selects enhanced framing on the DisplayPort ouput of this transcoder. **Locked once port is enabled. Updates when the port is disabled then re-enabled**

Value	Name	Description	Project
0b	Disable	Enhanced framing disabled	All
1b	Enable	Enhanced framing enabled	All

17:12	**Reserved** Project: All Format: MBZ
11:9	**Transcoder_DP_Bits_Per_Color** Project: All Default Value: 000b This field selects the number of bits per color output on DisplayPorts connected to this transcoder. Software should enable dithering in the pipe if selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer.

Value	Name	Description	Project
000b	8 bpc	8 bits per color	All
001b	10 bpc	10 bits per color	All
010b	6 bpc	6 bits per color	All
011b	12 bpc	12 bits per color	All
Others	Reserved	Reserved	All

8:5	**Reserved** Project: All Format: MBZ
4:3	**Transcoder_DP_Sync_Polarity** Project: All Default Value: 11b VS and HS are active high Indicates the polarity of Hsync and Vsync to be transmitted in MSA on this transcoder DisplayPort output.

Value	Name	Description	Project
00b	Low	VS and HS are active low (inverted)	All
01b	VS Low, HS High	VS is active low (inverted), HS is active high	All
10b	VS High, HS Low	VS is active high, HS is active low (inverted)	All
11b	High	VS and HS are active high	All

2:0	**Reserved** Project: All Format: MBZ

3.5 Analog Port CRT DAC

3.5.1 DAC_CTL—Analog Port CRT DAC Control

DAC_CTL

Register Type: MMIO
Project: All
Default Value: 00040000h
Access: R/W
Size (in bits): 32

Bit	Description
31	**Port_Enable** Project: All Default Value: 0b This bit enables or disables the analog port CRT DAC and syncs outputs.

Value	Name	Description	Project
0b	Disable	Disable the analog port DAC and disable output of syncs	All
1b	Enable	Enable the analog port DAC and enable output of syncs	All

Bit	Description
30:29	**Transcoder_Select** Project: All Default Value: 00b Determines which transcoder will feed this DAC port.

Value	Name	Description	Project
00b	Transcoder A	Transcoder A	All
01b	Transcoder B	Transcoder B	All
10b	Transcoder C	Transcoder C	All
11b	Reserved	Reserved	All

Bit	Description
28:26	**Reserved** Project: All Format:

DAC_CTL

25:24 **CRT_HPD_Channel_Status**

Project: All

Access: Read Only

Default Value: 00b

These bits are set when a CRT hot plug or unplug event has been detected and indicate which color channels were attached. Write a one to these bits to clear the status. The rising or falling edges of these bits are ORed together to go to the SDE_ISR CRT hot plug register bit.

Value	Name	Description	Project
00b	None	No channels attached	All
01b	Blue	Blue channel only is attached	All
10b	Green	Green channel only is attached	All
11b	Both	Both blue and green channel attached	All

23 **CRT_HPD_Enable**

Project: All

Default Value: 0b

Hot plug detection is used to set status bits or an interrupt on the connection or disconnection of a CRT to the analog port CRT DAC.

Value	Name	Description	Project
0b	Disable	CRT hot plug detection is disabled	All
1b	Enable	CRT hot plug detection is enabled	All

22 **CRT_HPD_Activation_Period**

Project: All

Default Value: 0b

This bit sets the activation period for the CRT hot plug circuit. [DevCPT] rawclk=125mhz

Value	Name	Description	Project
0b	64 rawclk	64 rawclk periods	All
1b	128 rawclk	128 rawclk periods	All

21 **CRT_HPD_Warmup_Time**

Project: All

Default Value: 0b

This bit sets the warmup time for the CRT hot plug circuit. [DevCPT] rawclk=125mhz

Value	Name	Description	Project
0b	4ms	Approximately 4ms	All
1b	8ms	Approximately 8ms	All

DAC_CTL

20 — **CRT_HPD_Sampling_Period**

Project: All

Default Value: 0b

This bit determines the length of time between sampling periods when the transcoder is disabled.

Value	Name	Description	Project
0b	2 seconds	Approximately 2 seconds	All
1b	4 seconds	Approximately 4 seconds	All

19:18 — **CRT_HPD_Voltage_Value**

Project: All

Default Value: 01b 50

Compare value for Vref to determine whether the analog port is connected to a CRT.

Value	Name	Description	Project
00b	40	40	All
01b	50	50 (Default)	All
10b	60	60	All
11b	70	70 (bit 17 must be = 1)	All

17 — **CRT_HPD_Reference_Voltage**

Project: All

Default Value: 0b

Value	Name	Description	Project
0b	325mv	325mv	All
1b	475mv	475mv (bits 19:18 must be = 11)	All

16 — **Force_CRT_HPD_Trigger**

Project: All

Default Value: 0b

Triggers a CRT hotplug/unplug detection cycle independent of the hot plug detection enable bit. This bit is automatically cleared after the detection is completed. The result of this trigger is reflected in the CRT Hot Plug Detection Status. Software must reset status after a force CRT detect trigger.

Value	Name	Description	Project
0b	No Trigger	No Trigger	All
1b	Force Trigger	Force Trigger	All

15:5 — **Reserved** Project: All Format:

DAC_CTL	
4	**VSYNC_Polarity_Control** Project: All Default Value: 0b The output VSYNC polarity is controlled by this bit. This is used to implement display modes that require inverted polarity syncs and to set the disabled state of the VSYNC signal. **Value** / **Name** / **Description** / **Project** 0b / Low / Active Low / All 1b / High / Active High / All
3	**HSYNC_Polarity_Control** Project: All Default Value: 0b The output HSYNC polarity is controlled by this bit. This is used to implement display modes that require inverted polarity syncs and to set the disabled state of the HSYNC signal. **Value** / **Name** / **Description** / **Project** 0b / Low / Active Low / All 1b / High / Active High / All
2:0	**Reserved** Project: All Format:

3.6 HDMI Port

3.6.1 HDMI_CTL—HDMI Port Control

HDMI_CTL	
Register Type:	MMIO
Project:	All
Default Value:	00000018h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Depends on bit

The operating mode (HDMI/DVI) of this port is determined by the setting of the encoding register field. **Ports C and D can only be used in HDMI/DVI mode.**

Note that DisplayPort B uses the same physical pins as HDMI/DVI B. Therefore HDMI/DVI B and DisplayPort B cannot be enabled simultaneously. The same applies for ports C and D.

Bit	Description
31	**Port_Enable** Project: All

Default Value: 0b

Disabling this port will put it in its lowest power state. Port enable takes place on the Vblank after being written. Both this bit and the audio output bit of this register must be enabled to send audio over this port.

Value	Name	Description	Project
0b	Disable	Disable and tristates the port interface	All
1b	Enable	Enables the port interface	All

30:29 **Transcoder_Select**

Project: All

Default Value: 00b

This bit determines from which display transcoder the source data will originate. Transcoder selection takes place on the Vblank after being written.

Value	Name	Description	Project
00b	Transcoder A	Transcoder A	All
01b	Transcoder B	Transcoder B	All
10b	Transcoder C	Transcoder C	All
11b	Reserved	Reserved	All

28:26 **Color_Format**

Project: All

Default Value: 000b

This field selects the number of bits per color sent to a receiver device connected to this port. Color format takes place on the Vblank after being written. Color format change must be done as a part of mode set since different color depths require different pixel clock settings.

Software should enable dithering in the pipe/transcoder if selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer.

Value	Name	Description	Project
000b	8 bpc	8 bits per color	All
011b	12 bpc	12 bits per color	All
Others	Reserved	Reserved	All

25 **Reserved**

Project: All

24 **Reserved** Project: All Format:

23 **Reserved**

Project: All

22:19 **Reserved** Project: All Format:

18 **Reserved**

Project: All

HDMI_CTL

17:16	**Reserved** Project: All Format:
15	**Port_Lane_Reversal** Project: All Default Value: 0b This bit reverses the order of the 4 lanes within the port. It is an OEM configurable feature. Locked once port is enabled. Updates when the port is disabled then re-enabled

Value	Name	Description	Project
0b	Not reversed	Not reversed	All
1b	Reversed	Reversed	All

14:12	**Reserved** Project: All Format:
11:10	**Encoding** Project: All Format: These bits select among encoding types. It is set as part of the display detection process. Control codes for ANSI 8b/10b and TMDS encoding must be programmed using these bits.

Value	Name	Description	Project
00b	Reserved		All
10b	TMDS	TMDS encoding for HDMI/DVI. See the HDMI specification for control codes. In this mode, the external HPD pin is used to generate hotplug.	All
Others	Reserved	Reserved	All

9	**HDMI_or_DVI_Select** Project: All Default Value: 0b This bit selects between HDMI and DVI modes of operation. HDMI mode enables a null packet (32 bytes of a value of 0) to be sent when Vsync=1 on this port, required for HDMI operation. It also enables preambles and guardbands prior to the null packets, in accordance with the HDMI specification. It is only valid for modes that use TMDS encoding.

Value	Name	Description	Project
0b	DVI	Port will function in DVI mode if no DIP packets are enabled and no audio is present.	All
1b	HDMI	Port will function in HDMI mode.	All

8	**Reserved** Project: All Format: MBZ
7	**Reserved** Project: All

HDMI_CTL

6 **Audio_Output_Enable**

Project: All

Default Value: 0b

This bit directs audio to this port. When enabled and audio data is available, the audio data will be combined with the video data and sent over this port. The audio unit uses the status of this bit to indicate presence of the HDMI output to the audio driver.

Value	Name	Description	Project
0b	Disable	No audio output on this port	All
1b	Enable	Enable audio on this port	All

5 **Reserved**

Project: All

4:3 **Sync_Polarity**

Project: All

Default Value: 11b VS and HS are active high

Indicates the polarity of Hsync and Vsync. Inverted polarity is transmitted as SYNC-BLANK-SYNC and standard polarity is transmitted as BLANK-SYNC-BLANK. For example, if Vsync is not inverted and Hsync is inverted, an Hsync period transmitted during Vsync would be transmitted as BLANK+VS+HS – BLANK+VS – BLANK+VS+HS.

Value	Name	Description	Project
00b	VS Low, HS Low	VS and HS are active low (inverted)	All
01b	VS Low, HS High	VS is active low (inverted), HS is active high	All
10b	VS High, HS Low	VS is active high, HS is active low (inverted)	All
11b	VS High, HS High	VS and HS are active high (Default)	All

2 **Port_Detected**

Project: All

Access: Read Only

Default Value: 0b

Read-only bit indicating whether a digital display was detected during initialization. It signifies the level of the GMBUS port (port 4 for B, port 3 for C, port 5 for D) data line at boot. This bit is valid regardless of whether the port is enabled.

Value	Name	Description	Project
0b	Not Detected	Port not detected during initialization	All
1b	Detected	Port detected during initialization	All

1:0 **Reserved** Project: All Format: MBZ

3.7 LVDS

3.7.1 LVDS—LVDS Port Control Register

LVDS—LVDS Port Control Register

Register Type: MMIO
Project: All
Default Value: 00000000h
Access: R/W Protect
Size (in bits): 32
Register Type: MMIO

Write Protect by Panel Power Sequencer

Bit	Description
31	**LVDS_Port_Enable** Project: All Default Value: 0b When disabled the LVDS port is inactive and in it's low power state. Enabling the LVDS port changes the way that the PLL for this transcoder is programmed. This bit must be set before the display PLL is enabled and the port is power sequenced on using the panel power sequencing logic. LVDS clockgating must be disabled (South Display Unit Clock Gating Disable bits #30, 14 in 0xC2020 set to '1') at boot and remained disabled before enabling dual channel LDVS mode.
30:29	**LVDS_Port_Transcoder_Select** Project: All Default Value: 1b Transcoder B
28:25	**Reserved** Project: All Format:

Value	Name	Description	Project
0b	Disable	The port is disabled and all LVDS pairs are powered down.	All
1b	Enable	The port is enabled (port must be enabled before powering up a connected panel)	All

Value	Name	Description	Project
0b	Transcoder A	The port gets data from Transcoder A	All
1b	Transcoder B	The port gets data from Transcoder B	All

LVDS—LVDS Port Control Register

24 **Data_Format_Select**

Project: All

Default Value: 0b

Combined with the other control bits it selects the LVDS data format. Other control bits in this register determine if two channel is enabled and 18 or 24 bit color is enabled.

Value	Name	Description	Project
0b	1x18.0, 2x18.0, 1x24.0 or 2x24.0	1x18.0, 2x18.0, 1x24.0 or 2x24.0	All
1b	1x24.1 or 2x24.1	1x24.1 or 2x24.1	All

23 **LE_Control_Enable**

Project: All

Default Value: 0b

This bit is used when the second channel control signal field indicates that we are using the LE instead of HS and the two channel mode is enabled. In single channel mode, this bit has no effect.

Value	Name	Description	Project
0b	Send 0	Send 0 on second channel HS (B2<2>)	All
1b	Send 1	Send 1 on second channel HS	All

22 **LF_Control_Enable**

Project: All

Default Value: 0b

This bit is used when the second channel control signal field indicates that we are using the LF instead of VS and two channel mode is enabled. In single channel mode, this bit has no effect.

Value	Name	Description	Project
0b	Send 0	Send 0 on second channel VS (B2<3>)	All
1b	Send 1	Send 1 on second channel VS	All

21 **VSYNC_Polarity**

Project: All

Default Value: 0b

This controls the polarity of the VSYNC indicator that is sent over the LVDS connection. Panels may require one or the other polarity or work with either polarity.

Value	Name	Description	Project
0b	No Invert	No inversion (1=active)	All
1b	Invert	Invert the sense (0=active)	All

LVDS—LVDS Port Control Register

20 **HSYNC_Polarity(LP_Invert)**

Project: All

Default Value: 0b

This controls the polarity of the HSYNC indicator that is sent over the LVDS connection. Panels may require one or the other polarity or work with either polarity.

Value	Name	Description	Project
0b	No Invert	No inversion (1=active)	All
1b	Invert	Invert the sense (0=active)	All

19 **DE_Invert**

Project: All

Default Value: 0b

This controls the polarity of the DE indicator that is sent over the LVDS connection.

Value	Name	Description	Project
0b	No Invert	No inversion of DE (1=active)	All
1b	Invert	Invert the sense of DE (0=active)	All

18:17 **Second_Channel_Control_Signals**

Project: All

Default Value: 00b

This bit only applies to the two channel modes of operation it has no effect in single channel modes.

Value	Name	Description	Project
00b		Send DE, HS, VS on second channel if enabled	All
01b	Reserved	Reserved	All
10b		Do not send DE, HS, VS on second channel use zero instead	All
11b		Use DE=0, HS=LE, VS=LF on second channel	All

16 **Channel_Reserved_Bits**

Project: All

Default Value: 0b

Value	Name	Description	Project
0b	Send 0	Send 0 for the channel reserved bits	All
1b	Send Duplicate	Send duplicate data bit for reserved bits	All

15:11 **Reserved** Project: All Format:

LVDS—LVDS Port Control Register

10

Buffer_Power_Down_State

Project: All

Default Value: 0b

This bit selects the state of the LVDS buffers during a powered down state caused by the power sequence logic power down. This selection will be made based on the connected panel requirements.

Value	Name	Description	Project
0b	Zero	Zero Volts (Driven on both lines of the pairs)	All
1b	Tri-State	Tri-State (High impedance state)	All

9:8

ClkA0_A2_Control

Project: All

Default Value: 00b

This field controls the A0-A2 data pairs and CLKA. It sets the highest level of activity that is allowed on these lines when the panel is powered on. Power sequencing for LVDS connected panels overrides the control. When the power sequencer is in the power down mode all signals are in the power down state.

Value	Name	Description	Project
00b	Power Down	Power Down all A channel signals including A3 (0V)	All
01b	Power Up Data 0	Power up – A0, A1, A2 Data bits forced to 0,Timing active, Clock Active	All
10b	Reserved	Reserved	All
11b	Power Up All Active	Power up – Data lines and clock active	All

7:6

Eight_bit_ch_A3_B3_Control

Project: All

Default Value: 00b

This field can control both the A3 and B3 data pairs. Enabling those pairs indicates the selection of 8-bit per color channel mode. It sets the highest level of activity that is allowed on these lines when the panel is powered on. The A3 pair will only be powered up if both this field and the A0, A1, A2, CLKA field indicates that the pair should be powered up and will only be active if both indicate that it should be active. The B3 pair will only be powered up if both this field and the B0, B1, B2, (B3) field indicates that the pair should be powered up and will only be active if both indicate that it should be active. Power sequencing for LVDS connected panels overrides the control. When the power sequencer is in the power down mode all signals are in the power down state.

Value	Name	Description	Project
00b	Power Down	Power Down all signals A3, B3 (common mode)	All
01b	Power Up Data 0	Power up – A3, (B3) Data (pixel data not control) lines forced to 0 output	All
10b	Reserved	Reserved	All
11b	Power Up Data Active	Power up – A3, (B3) Data lines active	All

LVDS—LVDS Port Control Register

5:4

Two_channel_mode_ClkB_Control

Project: All

Default Value: 00b

When in two channel mode, this field controls the CLKB pair. It sets the highest level of activity that is allowed on these lines when the panel is powered on. The CLKB pair should only be powered up if the B0, B1, B2, (B3) field indicates that the second channel should be powered up and will only be active if both indicate that it should be active. Power sequencing for LVDS connected panels overrides the control.

Value	Name	Description	Project
00b	Power Down	Power Down CLKB (common mode)	All
01b	Power Up CLKB 0	Power up – CLKB Forced to 0	All
10b	Reserved	Reserved	All
11b	Power Up CLKB Active	Power up – Clock B active	All

3:2

Two_channel_mode_B0_B2_Control

Project: All

Default Value: 00b

This field controls both the set B0-B2 data pairs. It sets the highest level of activity that is allowed on these lines when the panel is powered on. Power sequencing for LVDS connected panels overrides the control. During single channel operation (1x18.0), these bits need to be both zero. Two channel operation is selected by setting them to ones. Note that the second clock can be optionally enabled or disabled by the two channel mode ClkB control field.

Value	Name	Description	Project
00b	Power Down	Power Down all signals including B3 and CLKB	All
01b	Power Up Data 0	Power up – B0, B1, B2, Data lines forced to 0, timing is active	All
10b	Reserved	Reserved	All
11b	Power Up Data Active	Power up – Data lines active (color and timing)	All

1

Port_Detected

Project: All

Access: Read Only

Default Value: 0b

Read-only bit indicating whether LVDS was detected during initialization. It signifies the level of the GMBUS port 2 (LVDS) data line at boot. This bit is valid regardless of whether the port is enabled.

Value	Name	Description	Project
0b	Not Detected	LVDS not detected during initialization	All
1b	Detected	LVDS detected during initialization	All

0

Reserved Project: All Format:

3.8 DisplayPort

3.8.1 DP_CTL—DisplayPort Control

DP_CTL	
Register Type:	MMIO
Project:	All
Default Value:	00000018h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Depends on bit

Port enable is write protected by Panel Power Sequencer when panel is connected to this port.

Note that DisplayPort B uses the same physical pins as HDMI/DVI B. Therefore HDMI/DVI B and DisplayPort B cannot be enabled simultaneously. The same applies for ports C and D.

Bit	Description
31	**DisplayPort_Enable** Project: All Default Value: 0b Disabling this port will put it in its lowest power state. Port enable takes place on the Vblank after being written. **[DevCPT-A, DevCPT-B0]** When panel power sequencing is selected for DisplayPort D, the clock gating disable register SCLKGATE_DIS 0xC2020 bit 14 must be set to 1b prior to enabling DisplayPort D, then cleared to 0b after disabling DisplayPort D.
30:28	**Reserved** Project: All Format: MBZ
27:25	**Voltage_swing_level_set** Project: All Default Value: 0b These bits are used for setting the voltage swing for pattern 1, defined as Vdiff_pp in the DisplayPort specification.

Value	Name	Description	Project
0b	Disable	Disable and tristate the DisplayPort interface	All
1b	Enable	Enable the DisplayPort interface	All

Value	Name	Description	Project
000b	0.4V	0.4V	All
001b	0.6V	0.6V	All
010b	0.8V	0.8V	All
011b	1.2V	1.2V	All
Others	Reserved	Reserved	All

DP_CTL

24:22 **Preemphasis_level_set**

Project: All

Default Value: 0b

These bits are used for setting link pre-emphasis for pattern 2, as defined in the DisplayPort specification.

Value	Name	Description	Project
000b	0dB	No pre-emphasis	All
001b	3.5dB	3.5dB pre-emphasis (1.5x)	All
010b	6dB	6dB pre-emphasis (2x)	All
011b	9.5dB	9.5dB pre-emphasis (3x)	All
Others	Reserved	Reserved	All

21:19 **Port_Width_Selection**

Project: All

Default Value: 0b

This bit selects the number of lanes to be enabled on the DisplayPort link. Port width change must be done as a part of mode set. **Locked once port is enabled. Updates when the port is disabled then re-enabled.**

Value	Name	Description	Project
000b	x1	x1 Mode	All
001b	x2	x2 Mode	All
011b	x4	x4 Mode	All
Others	Reserved	Reserved	All

18:16 **Reserved** Project: All Format: MBZ

15 **Port_reversal**

Project: All

Default Value: 0b

Enables lane reversal within the port: lane 0 mapped to lane 3, lane 1 mapped to lane 2, etc. Port reversal does not affect AUX channel lane mapping.

Locked once port is enabled. Updates when the port is disabled then re-enabled

Value	Name	Description	Project
0b	Not Reversed	Port not reversed	All
1b	Reversed	Port reversed	All

14:11 **Reserved** Project: All Format: MBZ

DP_CTL

10:8 Link_training_pattern_enable

Project: All

Default Value: 0b

These bits are used for link initialization as defined in the DisplayPort specification. Please note that the link must first be configured prior to sending training patterns.

When enabling the port, it must be turned on with pattern 1 enabled. When retraining, the port must be disabled, then re-enabled with pattern 1 enabled.

Value	Name	Description	Project
000b	Pattern 1	Pattern 1 enabled: Repetition of D10.2 characters	All
001b	Pattern 2	Pattern 2 enabled: Repetition of K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2.	All
010b	Idle	Idle Pattern enabled: Transmit BS followed by VB-ID with NoVideoStream_flag set to 1, five times	All
011b	Normal	Link not in training: Send normal pixels	All
Others	Reserved	Reserved	All

7 Reserved

Project: All

6 Audio_Output_Enable

Project: All

Default Value: 0b

This bit enables audio output on this port. It may be enabled or disabled only when the link training is complete and set to "Normal".

Value	Name	Description	Project
0b	Disable	Audio output disabled	All
1b	Enable	Audio output enabled	All

5 Reserved

Project: All

4:3 Reserved Project: All Format: MBZ

DP_CTL	
2	**Port_Detected** Project: All Access: Read Only Default Value: 0b Read-only bit indicating whether a digital display was detected during initialization. It signifies the level of the detect pin (GMBUS port 4 for port B, GMBUS port 3 for port C, GMBUS port 5 for port D) at boot. This bit is valid regardless of whether the port is enabled. **Value** / **Name** / **Description** / **Project** 0b / Not Detected / Digital display not detected during initialization / All 1b / Detected / Digital display detected during initialization / All
1:0	**Reserved** Project: All Format: MBZ

3.8.2 DP_AUX_CTL—DisplayPort AUX Channel Control

DP_AUX_CTL	
Register Type: MMIO **Project:** All **Default Value:** 00050000h **Access:** R/W Special **Size (in bits):** 32	
Bit	**Description**
31	**Send_Busy** Project: All Default Value: 0b Setting this bit to a one initiates the transaction, when read this bit will be a 1 until the transmission completes. The transaction is completed when the response is received or when a timeout occurs. Do not write a 1 again until transaction completes. Writes of 0 will be ignored. **Programming Notes** Do not change any fields while Send/Busy bit 31 is asserted.
30	**Done** Project: All Access: R/W Clear A sticky bit that indicates the transaction has completed. SW must write a 1 to this bit to clear the event.
29	**Interrupt_on_Done** Project: All Format: Enable an interrupt in the hotplug status register when the transaction completes or times out.
28	**Time_out_error** Project: All Access: R/W Clear A sticky bit that indicates the transaction has timed out. SW must write a 1 to this bit to clear the event.

DP_AUX_CTL

27:26 — **Time_out_timer_value**

Project: All

Default Value: 00b

Used to determine how long to wait for receiver response before timing out.

Value	Name	Description	Project
00b	400us	400us	All
01b	600us	600us	All
10b	800us	800us	All
11b	1600us	1600us	All

25 — **Receive_error** Project: All Access: R/W Clear

A sticky bit that indicates that the data received was corrupted, not in multiples of a full byte, or more than 20 bytes. SW must write a 1 to this bit to clear the event.

24:20 — **Message_Size** Project: All Format:

This field is used to indicate the total number bytes to transmit (including the header). It also indicates the number of bytes received in a transaction (including the header). This field is valid only when the done bit is set, and if timeout or receive error has not occurred. Sync/Stop are not part of the message or the message size.

Reads of this field will give the response message size.

The read value will not be valid while Send/Busy bit 31 is asserted.

Message sizes of 0 or >20 are not allowed.

19:16 — **Precharge_Time** Project: All Format:

Default Value: 0101b 10us

Used to determine the precharge time for the Aux Channel drivers. During this time the Aux Channel will drive the SYNC pattern. Every microsecond gives one additional SYNC pulse beyond the hard coded 26 SYNC pulses.

The value is the number of microseconds times 2.

Default is 5 decimal which gives 10us of precharge which is 10 extra SYNC pulses for a total of 36.

Example:

For 10us precharge, program 5 (10us/2us).

15 — **Reserved**

Project: All

14 — **Reserved**

Project: All

13 — **Reserved**

Project: All

12 — **Reserved**

Project: All

DP_AUX_CTL	
11	**Reserved** Project: All
10:0	**2X_Bit_Clock_divider** Project: All Format: Used to determine the 2X bit clock the Aux Channel logic runs on. This value divides the input clock frequency down to 2X bit clock rate. It should be programmed to get as close as possible to the ideal rate of 2MHz. The input clock is the rawclk. [DevCPT] rawclk=125mhz Example: For 125MHz input clock and desired 2MHz 2X bit clock, program 63 (125MHz/2MHz).

3.8.3 DP_AUX_DATA—DisplayPort AUX Channel Data

DP Aux Channel Data Format	
Project:	All
Bit	**Description**
31:0	**AUX_CH_DATA** Project: All A DWord of the message. Writes give the data to transmit during the transaction. The MSbyte is transmitted first. Reads will give the response data after transaction complete.

DP_AUX_DATA						
Register Type:	MMIO					
Project:	All					
Default Value:	00000000h					
Access:	R/W					
Size (in bits):	5x32					
The read value will not be valid while the DisplayPort Aux Channel Control Register Send/Busy bit is asserted.						
DWord	**Bit**	**Description**				
0	31:0	**AUX_CH_DATA1**	Project:	All	Format:	DP Aux Channel Data Format
1	31:0	**AUX_CH_DATA2**	Project:	All	Format:	DP Aux Channel Data Format
2	31:0	**AUX_CH_DATA3**	Project:	All	Format:	DP Aux Channel Data Format
3	31:0	**AUX_CH_DATA4**	Project:	All	Format:	DP Aux Channel Data Format
4	31:0	**AUX_CH_DATA5**	Project:	All	Format:	DP Aux Channel Data Format

3.8.4 DP_BUFTRANS—DisplayPort Buffer Translation

DisplayPort Buffer Translation Format						
Project:	All					
Default Value:	00000000h					
Bit	**Description**					
31:28	**Reserved**	Project:	All	Format:	MBZ	
27:19	**OE** These bits select the OE vswing level	Project:	All	Range:	0..511	
18:17	**Reserved**	Project:	All	Format:	MBZ	
16:12	**Pre_Emphasis** These bits select the pre-emphasis level	Project:	All	Range:	0..31	
11:10	**Reserved**	Project:	All	Format:	MBZ	
9:6	**P_current_drive** These bits select the P current drive value	Project:	All	Range:	0..15	
5:4	**Reserved**	Project:	All	Format:	MBZ	
3:0	**N_current_drive** These bits select the N current drive value	Project:	All	Range:	0..15	

Programming Requirements:

DP mode		Offset	Value
L1	0dB	0xE4F00	**0x0100030C**
L1	3.5dB	0xE4F04	**0x00B8230C**
L1	6dB	0xE4F08	**0x06F8930C**
L1	9.5dB	0xE4F0C	**0x05F8E38E**
L2	0dB	0xE4F10	**0x00B8030C**
L2	3.5dB	0xE4F14	**0x0B78830C**
L2	6dB	0xE4F18	**0x09F8D3CF**
L3	0dB	0xE4F1C	**0x01E8030C**
L3	3.5dB	0xE4F20	**0x09F863CF**
L4	0 dB	0xE4F24	**0x0FF803CF**

Vswing	0dB pre-emphasis	3.5dB pre-emphasis	6dB pre-emphasis	9.5dB pre-emphasis
400mV	DWord 0	DWord 1	DWord 2	DWord 3
600mV	DWord 4	DWord 5	Dword 6	Not supported
800mV	Dword 7	Dword 8	Not supported	Not supported
1200mV	Dword 9	Not supported	Not supported	Not supported

DP_BUFTRANS

Register Type: MMIO
Project: All
Default Value: 0100038Eh; 00B8338Eh; 0178838Eh; 09F8E38Eh; 00B8038Eh; 0978838Eh; 09F8B38E; 0178038Eh; 09F8638Eh; 09F8038Eh
Access: R/W
Size (in bits): 10x32

These registers define current drive, pre-emphasis and voltage swing buffer programming required for the different voltage swing and pre-emphasis settings in the DisplayPort Control.

The default value is not the optimal value. See the programming requirements above for the correct values to use.

DWord	Bit	Description
0	31:0	**Vswing400mV_Pre0_0dB** Project: All Format: DisplayPort Buffer Translation Format See Description Above
1	31:0	**Vswing400mV_Pre3_5dB** Project: All Format: DisplayPort Buffer Translation Format See Description Above
2	31:0	**Vswing400mV_Pre6_0dB** Project: All Format: DisplayPort Buffer Translation Format See Description Above
3	31:0	**Vswing400mV_Pre9_5dB** Project: All Format: DisplayPort Buffer Translation Format See Description Above
4	31:0	**Vswing600mV_Pre0_0dB** Project: All Format: DisplayPort Buffer Translation Format See Description Above
5	31:0	**Vswing600mV_Pre3_5dB** Project: All Format: DisplayPort Buffer Translation Format See Description Above
6	31:0	**Vswing600mV_Pre6_0dB** Project: All Format: DisplayPort Buffer Translation Format See Description Above
7	31:0	**Vswing800mV_Pre0_0dB** Project: All Format: DisplayPort Buffer Translation Format See Description Above

DP_BUFTRANS			
8	31:0	**Vswing800mV_Pre3_5dB**	Project: All
		Format: DisplayPort Buffer Translation Format	See Description Above
9	31:0	**Vswing1200mV_Pre0_0dB**	Project: All
		Format: DisplayPort Buffer Translation Format	See Description Above

4. South Display Engine Audio

4.1 Audio Programming Sequence

The following HDMI and DisplayPort audio programming sequences are for use when enabling or disabling audio or temporarily disabling audio during a display mode set.

The audio codec and audio controller disable sequences must be followed prior to disabling the transcoder or port in a display mode set.

The audio codec and controller enable sequences can be followed after the transcoder is enabled and the port is enabled and completed link training (not sending TP1, TP2, or Idle).

The audio controller and audio codec sequences may be done in parallel or serial. In general, the change in ELDV/PD in the codec sequence will generate an unsolicited response to the audio controller driver to indicate that the controller sequence should start, but other mechanisms may be used.

Audio codec disable sequence:

- Disable sample fabrication
  - Set AUD_MISC_CTRL Sample_Fabrication_EN (bit 2) to “0”.
- Disable timestamps
  - Set AUD_CONFIG N_value_index (bit 29) to "0" for HDMI or "1" for DisplayPort.
  - Set N_programming_enable (bit 28) to "1"
  - Set Upper_N_value and Lower_N_value (bits 28:20, 15:4) to all "0"s.
- Disable ELDV and ELD buffer
  - Set AUD_CNTRL_ST2 ELD_valid (bit 0, 4, or 8 based on which port is used) to "0"
- Wait for 2 vertical blanks
- Optional: Disable audio PD (Presence Detect)
  - Software may choose to skip this in order to keep PD enabled during a resolution switch.
  - Set the port control register (HDMI_CTL or DP_CTL) Audio_Output_Enable (bit 6) to "0".

Audio controller disable sequence:

- Program Stream ID to 0 – Verb ID 706
- Disable audio info frames transmission – Verb ID 732
- Disable Digen – Verb ID 70D
- Program the codec to D3 state if needed.
- Audio driver may stop the audio controller DMA engine at this point if needed, but not required.

Audio codec enable sequence:

- Enable audio Presence Detect
  - Set the port control register (HDMI_CTL or DP_CTL) Audio_Output_Enable (bit 6) to "1".
- Wait for 1 vertical blank
- Load ELD buffer and Enable ELDV

- Set AUD_CNTRL_ST2 ELD_valid (bit 0, 4, or 8 based on which port is used) to "1".

- Enable timestamps
  - Set AUD_CONFIG N_value_index (bit 29) to "0" for HDMI or "1" for DisplayPort.
  - Set N_programming_enable (bit 28) to "0".
  - Program Upper_N_value and Lower_N_value (bits 28:20, 15:4) if a non-default N value is needed.
- Enable sample fabrication if this feature is needed
  - Set AUD_MISC_CTRL Sample_Fabrication_EN (bit 2) to “1”.

Audio controller enable sequence:

- Program the codec to D0 state if in D3 state.
- Program Stream ID to non zero – Verb ID 706
- Enable audio info frames transmission – Verb ID 732
- Enable Digen – Verb ID 70D
- If audio controller DMA engine is stopped, audio driver can start the DMA engine at this point.

4.2 Audio Configuration

4.2.1 AUD_CONFIG—Audio Configuration

AUD_CONFIG

Register Type: MMIO
Project: All
Default Value: 00000000h
Access: R/W
Size (in bits): 32

This register configures the audio output.

Bit	Description
31:30	**Reserved** Project: All Format:
29	**N_value_Index** Project: All Default Value: 0b

Value	Name	Description	Project
0b	HDMI	N value read on bits 27:20 and 15:4 reflects HDMI N value. Bits 27:20 and 15:4 are programmable to any N value – default h7FA6.	All
1b	Display Port	N value read on bits 27:20 and 15:4 reflects DisplayPort N value. Set this bit to 1 before programming N value register. When this bit is set to 1, 27:20 and 15:4 will reflect the current N value – default h8000.	All

28	**Reserved** Project: All

<table>
<tr><th colspan="2">AUD_CONFIG</th></tr>
<tr><td>27:20</td><td>Reserved Project: All</td></tr>
<tr><td>19:16</td><td>Pixel_Clock_HDMI
Project: All
Default Value: 0b
This is the target frequency of the CEA/HDMI video mode to which the audio stream is added. This value is used for generating N_CTS packets.
This refers to only HDMI Pixel clock and does not refer to DisplayPort Link clock. DisplayPort Link clock does not require this programming.
Note: The Transcoder on which audio is attached must be disabled when changing this field.
<table>
<tr><th>Value</th><th>Name</th><th>Description</th><th>Project</th></tr>
<tr><td>0000b</td><td>25.2 / 1.001 MHz</td><td>25.2 / 1.001 MHz</td><td>All</td></tr>
<tr><td>0001b</td><td>25.2 MHz</td><td>25.2 MHz (Program this value for pixel clocks not listed in this field)</td><td>All</td></tr>
<tr><td>0010b</td><td>27 MHz</td><td>27 MHz</td><td>All</td></tr>
<tr><td>0011b</td><td>27 * 1.001 MHz</td><td>27 * 1.001 MHz</td><td>All</td></tr>
<tr><td>0100b</td><td>54 MHz</td><td>54 MHz</td><td>All</td></tr>
<tr><td>0101b</td><td>54 * 1.001 MHz</td><td>54 * 1.001 MHz</td><td>All</td></tr>
<tr><td>0110b</td><td>74.25 / 1.001 MHz</td><td>74.25 / 1.001 MHz</td><td>All</td></tr>
<tr><td>0111b</td><td>74.25 MHz</td><td>74.25 MHz</td><td>All</td></tr>
<tr><td>1000b</td><td>148.5 / 1.001 MHz</td><td>148.5 / 1.001 MHz</td><td>All</td></tr>
<tr><td>1001b</td><td>148.5 MHz</td><td>148.5 MHz</td><td>All</td></tr>
<tr><td>Others</td><td>Reserved</td><td>Reserved</td><td>All</td></tr>
</table></td></tr>
<tr><td>15:4</td><td>Reserved Project: All</td></tr>
<tr><td>3</td><td>Disable_NCTS Project: All
Set this bit to disable N & CTS or M generation for CTM modes. This is to enable prediction of CRC in CTM modes.</td></tr>
<tr><td>2:0</td><td>Reserved Project: All Format:</td></tr>
</table>

4.2.2 AUD_CTS_ENABLE – Audio CTS Programming Enable

AUD_CTS_ENABLE

Register Type: MMIO
Project: All
Default Value: 00000000h
Access: Read Only
Size (in bits): 32

These values are returned from the device as the Subordinate Node Count response to a Get Root Node command.

Bit	Description
31:22	**Reserved** Project: All Format:
21	**CTS_M value Index** Project: All Default Value: 0b

Value	Name	Description	Project
0b	CTS	CTS value read on bits 23:4 reflects CTS value. Bit 23:4 is programmable to any CTS value. default is 0	All
1b	M	M value read on bits 21:4 reflects DisplayPort M value. Set this bit to 1 before programming M value register. When this is set to 1 23:4 will reflect the current N value	All

20	**Enable_CTS_or_M_programming** Project: All When set will enable CTS or M programming.
19:0	**CTS_programming** Project: All These are bits [19:0] of programmable CTS values for non-CEA modes. Bit 21 of this register must also be written in order to enable programming. Please note that the Transcoder to which audio is attached must be disabled when changing this field.

4.2.3 AUD_MISC_CTRL—Audio MISC Control

AUD_MISC_CTRL

Register Type: MMIO
Project: All
Default Value: 00000044h
Access: Read Only
Size (in bits): 32

Bit	Description
31:9	**Reserved** Project: All Format: MBZ
8	**Reserved** Project: All
7:4	**Output_Delay** Project: All Default Value: 0100b The number of samples between when the sample is received from the HD Audio link and when it appears as an analog signal at the pin.
3	**Reserved** Project: All Format: MBZ
2	**Sample_Fabrication_EN_bit** Project: All Access: R/W Default Value: 0b This bit indicates whether internal fabrication of audio samples is enabled during a link underrun.
1	**Pro_Allowed** Project: All Access: R/W Default Value: 0b By default, the audio device is configured to consumer mode and does not allow the mode to be changed to professional mode by an HD Audio verb. When Pro is allowed by setting this configuration bit, the HD Audio codec allows a verb to set the device into professional mode. Note: Setting this configuration bit does not change the default Pro bit value to be 1. Pro must be set to 1 through the normal process, using a verb.
0	**Reserved** Project: All Format: MBZ

Value	Name	Description	Project
0b	Disable	Audio fabrication disabled	All
1b	Enable	Audio fabrication enabled	All

Value	Name	Description	Project
0b	Consumer	Consumer use only	All
1b	Professional	Professional use allowed	All

4.2.4 AUD_VID_DID—Audio Vendor ID / Device ID

AUD_VID_DID	
Register Type:	MMIO
Project:	All
Default Value:	80862805h
Access:	Read Only
Size (in bits):	32

These values are returned from the device as the Vendor ID/ Device ID response to a Get Root Node command.

Bit	Description
31:16	**Vendor_ID** Project: All Format: Used to identify the codec within the PnP system. This field is hardwired within the device. Value = 0x8086
15:0	**Device_ID** Project: All Format: Constant used to identify the codec within the PnP system. This field is set by the device hardware. Value = 0x2805 [Cougarpoint]

4.2.5 AUD_RID—Audio Revision ID

AUD_RID	
Register Type:	MMIO
Project:	All
Default Value:	00100000h
Access:	Read Only
Size (in bits):	32

These values are returned from the device as the Revision ID response to a Get Root Node command.

Bit	Description
31:24	**Reserved** Project: All Format:
23:20	**Major_Revision** Project: All Default Value: 0001b The major revision number (left of the decimal) of the HD Audio Spec to which the codec is fully compliant. This field is hardwired within the device. Value = 0x1
19:16	**Minor_Revision** Project: All The minor revision number (rights of the decimal) or “dot number” of the HD Audio Spec to which the codec is fully compliant. This field is hardwired within the device. Value = 0x0
15:8	**Revision_ID** Project: All The vendor’s revision number for this given Device ID. This field is hardwired within the device. Value = 0x0

AUD_RID	
7:0	**Stepping_ID** Project: All An optional vendor stepping number within the given Revision ID. This field is hardwired within the device. Value = 0x0

4.2.6 AUD_PWRST—Audio Power State

Audio Power State Format	
Project:	All
Bit	**Description**
1:0	**Power_State** Project: All Default Value: 11b D3

Value	Name	Description	Project
00b	D0	D0	All
01b,10b	Unsupported	Unsupported	All
11b	D3	D3	All

AUD_PWRST	
Register Type:	MMIO
Project:	All
Default Value:	00FFFFFFh
Access:	Read Only
Size (in bits):	32

These values are returned from the device as the Power State response to a Get Audio Function Group command.

Bit	Description
31:28	**Reserved** Project: All Format:
27:26	**Func_Grp_Dev_PwrSt_Curr** Project: All Format: Audio Power State Format Function Group Device current power state
25:24	**Func_Grp_Dev_PwrSt_Set** Project: All Format: Audio Power State Format Function Group Device power state that was set
23:22	**ConvC_Widget_PwrSt_Curr** Project: All Format: Audio Power State Format ConverorC Widget current power state

AUD_PWRST						
21:20	**ConvC_Widget_PwrSt_Req** ConverorC Widget power state that was requested by audio software	Project:	All	Format:	Audio Power State Format
19:18	**ConvertorB_Widget_PwrSt_Curr** ConverorB Widget current power state	Project:	All	Format:	Audio Power State Format
17:16	**ConvertorB_Widget_PwrSt_Req** ConverorB Widget power state that was requested by audio software	Project:	All	Format:	Audio Power State Format
15:14	**ConvertorA_Widget_PwrSt_Curr** ConverorA Widget current power state	Project:	All	Format:	Audio Power State Format
13:12	**ConvertorA_Widget_PwrSt_Req** ConverorA Widget power state that was requested by audio software	Project:	All	Format:	Audio Power State Format
11:10	**PinD_Widget_PwrSt_Curr** PinD Widget current power state	Project:	All	Format:	Audio Power State Format
9:8	**PinD_Widget_PwrSt_Set** PinD Widget power state that was set	Project:	All	Format:	Audio Power State Format
7:6	**PinC_Widget_PwrSt_Curr** PinC Widget current power state	Project:	All	Format:	Audio Power State Format
5:4	**PinC_Widget_PwrSt_Set** PinC Widget power state that was set	Project:	All	Format:	Audio Power State Format
3:2	**PinB_Widget_PwrSt_Curr** PinB Widget current power state	Project:	All	Format:	Audio Power State Format
1:0	**PinB_Widget_PwrSt_Set** PinB Widget power state that was set	Project:	All	Format:	Audio Power State Format

4.2.7 AUD_PINW_CONNLNG_LIST—Audio Connection List

AUD_PINW_CONNLNG_LIST	
Register Type:	MMIO
Project:	All
Default Value:	00000302h
Access:	Read Only
Size (in bits):	32

These values are returned from the device as the Connection List Length response to a Get Pin Widget command.

Bit	Description
31:16	**Reserved** Project: All Format:
15:8	**Connection_List_Entry** Project: All Default Value: 03h Connection to Convertor Widget Node 0x03
7	**Long_Form** Project: All Default Value: 0b This bit indicates whether the items in the connection list are ‘long form’ or ‘short form’. This bit is hardwired to 0 (items in connection list are short form)
6:0	**Connection_List_Length** Project: All Default Value: 02h This field indicates the number of items in the connection list. If this field is 2, there is only one hardwired input possible, which is read from the Connection List, and there is no Connection Select Control.

4.2.8 AUD_PINW_CONNLNG_SEL—Audio Connection Select

AUD_PINW_CONNLNG_SEL	
Register Type:	MMIO
Project:	All
Default Value:	00000000h
Access:	Read Only
Size (in bits):	32

These values are returned from the device as the Connection List Length response to a Get Pin Widget command.

Bit	Description
31:24	**Reserved** Project: All Format:
23:16	**Connection_select_Control_D** Project: All Format: Connection Index Currently Set [Default 0x00], Port D Widget is set to 0x00
15:8	**Connection_select_Control_C** Project: All Format: Connection Index Currently Set [Default 0x00], Port C Widget is set to 0x00

AUD_PINW_CONNLNG_SEL	
7:0	**Connection_select_Control_B** Project: All Format: Connection Index Currently Set [Default 0x00], Port B Widget is set to 0x00

4.2.9 AUD_CNTL_ST—Audio Control State

AUD_CNTL_ST	
Register Type:	MMIO
Project:	All
Default Value:	00005400h
Access:	R/W
Size (in bits):	32

Bit	Description
31	**Reserved** Project: All Format: MBZ
30:29	**DIP_Port_Select** Project: All Access: Read Only Default Value: 00b This read-only bit reflects which port is used to transmit the DIP data. This can only change when DIP is disabled. If one or more audio-related DIP packets is enabled and audio is enabled on a digital port, these bits will reflect the digital port to which audio is directed.
28:25	**Reserved** Project: All Format: MBZ

Value	Name	Description	Project
00b	Reserved	Reserved	All
01b	Digital Port B	Digital Port B	All
10b	Digital Port C	Digital Port C	All
11b	Digital Port D	Digital Port D	All

AUD_CNTL_ST

24:21 **DIP_type_enable_status**

Project: All

Access: Read Only

Default Value: 0000b

These bits reflect the DIP types enabled. It can be updated while the port is enabled. Within 2 vblank periods, the DIP is guaranteed to have been transmitted. Disabling a DIP type results in setting the contents of that DIP buffer to zero. A reserved setting reflects a disabled DIP.

Value	Name	Description	Project
XXX0b	Disable	Audio DIP disabled	All
XXX1b	Enable	Audio DIP enabled	All
XX0Xb	Disable	Generic 1 (ACP) DIP disabled	All
XX1Xb	Enable	Generic 1 (ACP) DIP enabled	All
X0XXb	Disable	Generic 2 DIP disabled	All
X1XXb	Enable	Generic 2 DIP enabled, can be used by ISRC1 or ISRC2	All
1XXXb	Reserved	Reserved	All

20:18 **DIP_buffer_index**

Project: All

Default Value: 0000b

This field is used during read of different DIPs, and during read or write of ELD data. These bits are used as an index to their respective DIP or ELD buffers. When the index is not valid, the contents of the DIP will return all 0's.

Value	Name	Description	Project
000b	Audio	Audio DIP (31 bytes of address space, 31 bytes of data)	All
001b	Gen 1	Generic 1 (ACP) Data Island Packet (31 bytes of address space, 31 bytes of data)	All
010b	Gen 2	Generic 2 (ISRC1) Data Island Packet (31 bytes of address space, 31 bytes of data)	All
011b	Gen 3	Generic 3 (ISRC2) Data Island Packet (31 bytes of address space, 31 bytes of data)	All
Others	Reserved	Reserved	All

AUD_CNTL_ST

17:16 DIP_transmission_frequency

Project: All

Access: Read Only

Default Value: 00b

These bits reflect the frequency of DIP transmission for the DIP buffer type designated in bits 20:18. When writing DIP data, this value is also latched when the first DW of the DIP is written.

When read, this value reflects the DIP transmission frequency for the DIP buffer designated in bits 20:18.

Value	Name	Description	Project
00b	Disable	Disabled	All
01b	Reserved	Reserved	All
10b	Send Once	Send Once	All
11b	Best Effort	Best effort (Send at least every other vsync)	All

15 Reserved Project: All Format: MBZ

14:10 ELD_buffer_size Project: All Access: Read Only

10101 = This field reflects the size of the ELD buffer in DWORDs (84 Bytes of ELD)

9:5 ELD_access_address Project: All

Selects the DWORD address for access to the ELD buffer (84 bytes). The value wraps back to zero when incremented past the max addressing value 0x1F. This field change takes effect immediately after being written. The read value indicates the current access address.

4 ELD_ACK Project: All

Acknowledgement from the audio driver that ELD read has been completed

3:0 DIP_access_address Project: All

Selects the DWORD address for access to the DIP buffers. The value wraps back to zero when it incremented past the max addressing value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.

4.2.10 AUD_CNTRL_ST2— Audio Control State 2

AUD_CNTRL_ST2	
Register Type:	MMIO
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

This register is used for handshaking between the audio and video drivers for interrupt management. For each port, ELD and content protection readiness is sent by the display software to the audio software via an unsolicited response when the ELD or CP ready bit is set. Display software sets these bits as part of enabling the respective audio-enabled digital port.

Bit	Description
31:10	**Reserved** Project: All Format:
9	**CP_ReadyD** Project: All Default Value: 0b This **R/W** bit reflects the state of CP request from the audio unit. When an audio CP request has been serviced, it must be reset to 1 by the video software to indicate that the CP request has been serviced.
8	**ELD_validD** Project: All Default Value: 0b This **R/W** bit reflects the state of the ELD data written to the ELD RAM. After writing the ELD data, the video software must set this bit to 1 to indicate that the ELD data is valid. At audio codec initialization, or on a hotplug event, this bit is set to 0 by the video software. This bit is reflected in the audio pin complex widget as the ELD valid status bit.
7:6	**Reserved** Project: All Format:

Value	Name	Description	Project
0b	Pending or Not Ready	CP request pending or not ready to receive requests	All
1b	Ready	CP request ready	All

Value	Name	Description	Project
0b	Invalid	ELD data invalid (default, when writing ELD data, set 0 by software)	All
1b	Valid	ELD data valid (Set by video software only)	All

AUD_CNTRL_ST2

5 **CP_ReadyC**

Project: All

Default Value: 0b

See CP_ReadyD description.

Value	Name	Description	Project
0b	Not Ready	CP request pending or not ready to receive requests	All
1b	Ready	CP request ready	All

4 **ELD_validC**

Project: All

Default Value: 0b

See ELD_validD descripion.

Value	Name	Description	Project
0b	Invalid	ELD data invalid (default, when writing ELD data, set 0 by software)	All
1b	Valid	ELD data valid (Set by video software only)	All

3:2 **Reserved** Project: All Format:

1 **CP_ReadyB**

Project: All

Default Value: 0b

See CP_ReadyD description.

Value	Name	Description	Project
0b	Not Ready	CP request pending or not ready to receive requests	All
1b	Ready	CP request ready	All

0 **ELD_validB**

Project: All

Default Value: 0b

See ELD_validD descripion.

Value	Name	Description	Project
0b	Invalid	ELD data invalid (default, when writing ELD data, set 0 by software)	All
1b	Valid	ELD data valid (Set by video software only)	All

4.2.11 AUD_HDMIW_HDMIEDID—Audio HDMI Data EDID Block

AUD_HDMIW_HDMIEDID	
Register Type:	MMIO
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32

These registers contain the HDMI data block from the EDID. The graphics driver reads the EDID and writes the structure to these registers. The vendor specific data block may be longer than 8 bytes, but the driver must not write more than 48 bytes to the buffer. The EDID format is Version 3 within the CEA-861B specification. The HDMI Vendor Specific Data Block is described in version 1.1 of the HDMI specification.

These values are returned from the device as the HDMI Vendor Specific Data Block response to a Get HDMI Widget command.

Writing sequence:

- Video software sets ELD invalid, and sets the ELD access address to 0, or to the desired DWORD to be written.
- Video software writes ELD data 1 DWORD at a time. The ELD access address autoincrements with each DWORD write, wrapping around to address 0 when the max buffer address size of 0xF has been reached. Please note that software must write an entire DWORD at a time.
- Please note that the audio driver checks the valid bit with each byte read of the ELD. This means that the video driver can unilaterally write ELD irrespective of audio driver ELD read status.

Reading sequence:

- Video software sets the ELD access address to 0, or to the desired DWORD to be read.
- Video software reads ELD data 1 DWORD at a time. The ELD access address autoincrements with each DWORD read, wrapping around to address 0 when the max buffer address size of 0xF has been reached.

Bit	Description
31:0	**EDID_HDMI_Data_Block** Project: All Format: Please note that the contents of this buffer are not cleared when ELD is disabled. The contents of this buffer are cleared during gfx reset

4.2.12 AUD_HDMIW_INFOFR—Audio Widget Data Island Packet

AUD_HDMIW_INFOFR	
Register Type:	MMIO
Project:	All
Default Value:	00000000h
Access:	Read Only
Size (in bits):	32

When the IF type or dword index is not valid, the contents of the DIP will return all 0's.

These values are programmed by the audio driver in an HDMI Widget Set command. They are returned one byte at a time from the device on the HD audio bus as the HDMI DIP response to a Get HDMI Widget command. To fetch a specific byte, the audio driver should send an HDMI Widget HDMI DIP Index Pointer Set command to set the index, then fetch the indexed byte using the HDMI DIP get.

Bit	Description
31:0	**Data_Island_Packet_Data** Project: All Format: This reflects the contents of the DIP indexed by the DIP access address. The contents of this buffer are cleared during function reset or HD audio link reset.

5. South Display Engine Transcoder and FDI Control

5.1 Transcoder Control

5.1.1 TRANS_CONF—Transcoder Configuration

TRANS_CONF	
Register Type:	MMIO
Project:	All
Default Value:	00000000h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Start of vertical blank OR transcoder disabled

Bit	Description
31	**Transcoder_Enable** Project: All Setting this bit to the value of one, turns on the transcoder. Turning the transcoder off disables the timing generator and synchronization pulses to the display will not be maintained. Transcoder timing registers must contain valid values before this bit is enabled. **Value** / **Name** / **Description** / **Project** 0b / Disable / Disabled / All 1b / Enable / Enabled / All
30	**Transcoder_State** Project: All This **read only** bit indicates the actual state of the transcoder. Since there can be some delay between disabling the transcoder and the transcoder actually shutting off, this bit indicates the true current state of the transcoder. **Value** / **Name** / **Description** / **Project** 0b / Disabled / Transcoder is disabled / All 1b / Enabled / Transcoder is enabled / All
29:24	**Reserved** Project: All Format:

TRANS_CONF

23:21 Interlaced_Mode

Project: All

Default Value: 000b

These bits are used for control of the transcoder interlaced mode.

Value	Name	Description	Project
000b	Progressive	Progressive	All
011b	Interlaced	Interlaced (north display must also be set to interlaced)	All
Others	Reserved	Reserved	All

20:11 Reserved Project: All Format:

10 xvYCC_Color_Range_Limit

Project: All

Default Value: 0b

This bit is used to limit the color range of the port outputs from 1 to 254 for 8-bit components, 4 to 109 for 10-bit components, or 16 to 4079 for 12-bit components. Values outside of the range will be clamped to fit within the range. There is no need to set this bit if the equivalent bit is set in the north display pipe configuration register.

Value	Name	Description	Project
0b	Full	Do not limit the range	All
1b	Limit	Limit range	All

9:0 Reserved Project: All Format:

5.2 FDI Receiver

5.2.1 FDI_RX_CTL— FDI Rx Control

FDI_RX_CTL

Register Type:	MMIO
Project:	All
Default Value:	00000040h
Access:	R/W
Size (in bits):	32
Double Buffer Update Point:	Depends on bit

Bit	Description
31	**FDI_Rx_Enable** Project: All Default Value: 0b Disabling this port will put it in its lowest power state. Port enable takes place on the Vblank after being written.

Value	Name	Description	Project
0b	Disable	Disable and tristate the FDI Rx interface	All
1b	Enable	Enable the FDI Rx interface	All

Bit	Description
30:28	**Reserved** Project: All Format: MBZ
27	**FS_error_correction_enable** Project: All Default Value: 0b This bit enables the Fill Start error correction over FDI. Once the FS code is incorrectly received, the receiver will recover the FS code. The FDI Rx TU size register must be set correctly. The following condition must be met in order to set this bit: **(Active+2)/TU >= 1**

Value	Name	Description	Project
0b	Disable	Disable FS Error Correction	All
1b	Enable	Enable FS Error Correction	All

FDI_RX_CTL

26 — **FE_error_correction_enable**

Project: All

Default Value: 0b

This bit enables the Fill End error correction over FDI. Once the FE code is incorrectly received, the receiver will recover the FE code. The FDI Rx TU size register must be set correctly. The following condition must be met in order to set this bit: **(Active+2)/TU >= 1**

Value	Name	Description	Project
0b	Disable	Disable FE Error Correction	All
1b	Enable	Enable FE Error Correction	All

25 — **FS_error_reporting_enable**

Project: All

Default Value: 0b

This bit enables the FS error reporting over FDI. Once the FS code is incorrectly received, the receiver will report the FS code error through an interrupt. The FDI Rx TU size register must be set correctly. The following condition must be met in order to set this bit: **(Active+2)/TU >= 1**

Value	Name	Description	Project
0b	Disable	Disable FS Error Reporting	All
1b	Enable	Enable FS Error Reporting	All

24 — **FE_error_reporting_enable**

Project: All

Default Value: 0b

This bit enables the FE error reporting over FDI. Once the FE code is incorrectly received, the receiver will report the FE code error through an interrupt. The FDI Rx TU size register must be set correctly. The following condition must be met in order to set this bit: **(Active+2)/TU >= 1**

Value	Name	Description	Project
0b	Disable	Disable FE Error Reporting	All
1b	Enable	Enable FE Error Reporting	All

23:22 — **Reserved** Project: All Format:

FDI_RX_CTL

21:19 **Port_Width_Selection**

Project: All

Default Value: 0b

These bits select the number of lanes to be enabled on the link. Port width change must be done as a part of mode set.

[DevCPT] FDI B and FDI C share lanes. FDI C maximum port width is 2 lanes. FDI B maximum port width is 4 lanes when FDI C is disabled, 2 lanes when FDI C is enabled.

Locked once port is enabled. Updates when the port is disabled then re-enabled

Value	Name	Description	Project
000b	x1 Mode	x1 Mode	All
001b	x2 Mode	x2 Mode	All
010b	x3 Mode	x3 Mode	All
011b	x4 Mode	x4 Mode	All
Others	Reserved	Reserved	All

18:16 **Bits_Per_Color**

Project: All

Default Value: 0b

This field selects the number of bits per color sent over the link. Color format takes place on the Vblank after being written.

Value	Name	Description	Project
000b	8 bpc	8 bits per color	All
001b	10 bpc	10 bits per color	All
010b	6 bpc	6 bits per color	All
011b	12 bpc	12 bits per color	All
Others	Reserved	Reserved	All

15 **Link_reversal_strap_override**

Project: All

Default Value: 0b

Link is reversed if DMI is reversed. This bit overrides the status of DMI reversal to the reverse of what is strapped. It must be set before the link is enabled in order to take effect. Writing to this bit when the link is enabled has no effect. All FDI links must be off in order for this bit to take effect. This bit is ORed with the link reversal strap overrides from any other FDI Rx Control registers.

Value	Name	Description	Project
0b	Not Overwritten	Link reversal strap not overwritten	All
1b	Overwritten	Link reversal strap overwritten.	All

FDI_RX_CTL

14 **DMI_Link_reversal_status**

Project: All

Access: Read Only

Default Value: 0b

This bit reflects the DMI link reversal strap.

Value	Name	Description	Project
0b	Not Reversed	Link not reversed	All
1b	Reversed	Link reversed.	All

13 **FDI_PLL_enable** Project: All Format: Enable

This bit enables the FDI PLL. After enabling the FDI PLL, software must wait for a warmup period after before enabling the link. This bit is ORed with the FDI PLL enables from any other FDI Rx Control registers.

12 **Reserved** Project: All Format:

11 **Composite_Sync_Select**

Project: All

Default Value: 0b

This bit selects between composite Sync and separate Fsync/Lsync on this port. Composite sync must be used when three pipes are enabled.

Value	Name	Description	Project
0b	Separate	Separate Fsync/Lsync	All
1b	Composite	Composite Sync	All

10 **FDI_Auto_Train**

Project: All

Default Value: 0b

This bit enables FDI auto-training on this port. Locked once port is enabled. Updates when port is disabled.

Value	Name	Description	Project
0b	Disable	Disable FDI auto-training	All
1b	Enable	Enable FDI auto-training	All

FDI_RX_CTL

9:8 Link_training_pattern_enable

Project: All

Default Value: 0b

These bits are used for link initialization. Please note that the link must first be configured prior to sending training patterns

When enabling the port, it must be turned on with pattern 1 enabled. When retraining, the port must be disabled, then re-enabled with pattern 1 enabled.

Value	Name	Description	Project
00b	Pattern 1	Pattern 1 enabled: Repetition of D10.2 characters.	All
01b	Pattern 2	Pattern 2 enabled: Repetition of K28.5, D11.6, K28.5, D11.6, D10.2, D10.2, D10.2, D10.2, D10.2, D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2.	All
10b	Idle	Idle Pattern enabled: Transmit BS followed by VB-ID with NoVideoStream_flag set to 1, five times	All
11b	Normal	Link not in training: Send normal pixels	All

7 Reserved

Project: All

6 Enhanced_Framing_Enable

Project: All

Default Value: 1b Enhanced framing enabled

This bit selects enhanced framing.

Locked once port is enabled. Updates when the port is disabled then re-enabled

Value	Name	Description	Project
0b	Disable	Enhanced framing disabled	All
1b	Enable	Enhanced framing enabled	All

5 Reserved

Project: All

FDI_RX_CTL	
4	**Rawclk_to_PCDCLK_selection** Project: All Default Value: 0b This bit switches PCH display clocking between the raw oscillator clock ([DevCPT] rawclk=125mhz)and PCDCLK ([DevCPT] PCDCLK=450mhz). It must be programmed as part of enabling and disabling the link. Please see the mode set / boot flow for more detail. This bit is ORed with the selection bit from any other FDI Rx Control registers. **Value** / **Name** / **Description** / **Project** 0b / Rawclk / Rawclk used / All 1b / PCDCLK / PCDCLK used / All
3:0	**Reserved** Project: All Format: MBZ

5.2.2 FDI_RX_MISC— FDI Rx Miscellaneous

FDI_RX_MISC	
Register Type: MMIO **Project:** All **Default Value:** 00000080h **Access:** R/W **Size (in bits):** 32	
Bit	**Description**
31:22	**Reserved** Project: All Format: MBZ
21:20	**TP1_to_TP2_Time** Project: All Default Value: 0b These bits select the number of link clocks to count before transitioning from TP1 to TP2 during auto training. Program to 48 clocks before enabling FDI with auto-training. **Value** / **Name** / **Description** / **Project** 10b / 48 / 48 clocks - **required programming** / All 11b / 64 / 64 clocks / All
19	**Reserved** Project: All Format: MBZ

FDI_RX_MISC	
18:16	**Bit_Lock_Timeout_Time** Project: All Default Value: 0b These bits select the number of link clocks to count before timing out on bit lock during auto training.

Value	Name	Description	Project
000b	128	128 clocks	All
001b	256	256 clocks	All
010b	384	384 clocks	All
011b	512	512 clocks	All
100b	640	640 clocks	All
101b	768	768 clocks	All
110b	896	896 clocks	All
111b	1024	1024 clocks	All

15:13	**Reserved** Project: All Format: MBZ
12:0	**FDI_Delay** Project: All Default Value: 80h Default 80h. This field specifies latency as relative delay with respect to the dot clock required for active data over the FDI interface to reach the timing generator FIFO in the transcoder.

5.2.3 FDI_RX_IMR — FDI Rx Interrupt Mask

FDI Receiver Interrupt Bit Definition	
Project: All	
FDI Receiver (FDI Rx) interrupt bits come from FDI Receiver events. The FDI_RX_IIR bits are ORed together to generate the FDI_RX Combined Interrupt which will appear in the South Display Engine Interrupt Control Registers. The FDI Receiver Interrupt Control Registers all share the same bit definitions from this table.	
Bit	**Description**
31:12	**Reserved** Project: All Format:
11	**FDI_RX_Bit_Lock_Timeout** Project: All Format: This indicates that bit lock timeout occured.
10	**FDI_RX_Interlane_Alignment** Project: All Format: This indicates all the lanes are properly inter-lane aligned.
9	**FDI_RX_Symbol_Lock** Project: All Format: This indicates training pattern 2 was consecutively received successfully on all the enabled lanes.
8	**FDI_RX_Bit_Lock** Project: All Format: This indicates D10.2 pattern in training pattern 1 was consecutively received successfully on all the enabled lanes.

FDI Receiver Interrupt Bit Definition				
7	**FDI_RX_Training_Pattern_2_Fail** This indicates that the training pattern 2 has failed.	Project:	All	Format:
6	**FS_Code_Error** This reports the Fill Start code missing condition.	Project:	All	Format:
5	**FE_Code_Error** This reports the Fill End code missing condition.	Project:	All	Format:
4	**FDI_RX_High_Symbol_Error_Rate** This indicates the received symbol error rate is more than 10^-10.	Project:	All	Format:
3	**Reserved**	Project:	All	Format:
2	**FDI_RX_Pixel_FIFO_Overflow**	Project:	All	Format:
1	**FDI_RX_Cross_Clock_FIFO_Overflow** This indicates the cross clock symbol clock to display clock FIFO overflowed.	Project:	All	Format:
0	**FDI_RX_Symbol_Queue_overflow** This indicates the symbol queue overflowed.	Project:	All	Format:

FDI_RX_IMR

Register Type: MMIO
Project: All
Default Value: 000007FFh
Access: R/W
Size (in bits): 32

See the interrupt bit definition table to find the source event for each interrupt bit.

Bit	Description
31:0	**Interrupt_Mask_Bits** Project: All This field contains a bit mask which selects which FDI_RX events are reported int the FDI_RX_IIR.

Value	Name	Description	Project
0b	Not Masked	Not Masked – will be reported in the FDI_RX_IIR	All
1b	Masked	Masked – will not be reported in the FDI_RX_IIR	All

5.2.4 FDI_RX_IIR — FDI Rx Interrupt Identity

FDI_RX_IIR	
Register Type:	MMIO
Project:	All
Default Value:	00000000h
Access:	R/W Clear
Size (in bits):	32

See the interrupt bit definition table to find the source event for each interrupt bit.

Bit	Description
31:0	**Interrupt_Identity_Bits** Project: All This field holds the persistent values of the FDI_RX interrupt bits which are unmasked by the FDI_RX_IMR. Bits set in this register will propagate to the combined FDI_RX interrupt in the SDE_ISR. Bits set in this register will remain set (persist) until the interrupt condition is cleared by writing a '1' to the appropriate bits.

Value	Name	Description	Project
0b	Condition Not Detected	Interrupt Condition Not Detected	All
1b	Condition Detected	Interrupt Condition Detected	All

5.2.5 FDI_RX_TUSIZE— FDI Rx Transfer Unit Size

The FDI Receiver TU1 and TU2 sizes must be programmed to match the TU sizes used by the FDI Transmitter.

When switching between two refresh rates, both the TU1 and TU2 values must be programmed. For dynamic refresh rate control, TU1 values are the primary values and are used for the normal setting, and TU2 values are the secondary values and are used for the lower power setting.

FDI_RX_TUSIZE	
Register Type:	MMIO
Project:	All
Default Value:	7E000000h
Access:	R/W
Size (in bits):	32

Bit	Description
31	**Reserved** Project: All Format: MBZ
30:25	**TU_Size** Project: All This field is the size of the transfer unit for FDI, minus one.
24:0	**Reserved** Project: All Format: MBZ

Revision History

Revision Number	Description	Revision Date
1.0	First 2011 OpenSource edition	May 2011

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